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Citation: Review of Scientific Instruments **32**, 189 (1961); doi: 10.1063/1.1717307
View online: http://dx.doi.org/10.1063/1.1717307
View Table of Contents: http://scitation.aip.org/content/aip/journal/rsi/32/2?ver=pdfcov
Published by the AIP Publishing

Transistorized Electronic Analog Multiplier

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(Received April 4, 1960; and in final form, September 29, 1960)

The exponential current-voltage characteristic of the input of a grounded base junction transistor is utilized to construct an analog multiplier. Four-quadrant operation is obtained by using two channels—one with pnp and the other with npn transistors. Design considerations of the various components of the multiplier are discussed. It is shown that the performance of the multiplier—particularly in respect of bandwidth—compares favorably with that of the other types described in the literature.

INTRODUCTION

DESIGN and development of a satisfactory multiplier unit have been a problem of considerable investigation and research in electronic analog computer technique. The possibility of the use of a transistor as an analog multiplier by using the nonlinear nature of the input resistance has been suggested by Chaplin and Owens.[1] The authors of the present note investigated[2] the probable operating characteristics of such a multiplier and showed that it should be possible to design a multiplier in such a manner as to obtain an accurate law of response over a wide range of input signal, a substantially large bandwidth, and a reasonably low thermal drift. Further, as is usual with transistorized equipment, it should have the additional desirable feature of compactness and, since the product appears as a modulated sinusoidal current, the necessity for using a chopper or a dc amplifier for subsequent amplification does not arise with the equipment. A practical multiplier unit possessing most of these features has been designed and is described here. For the sake of completeness the principle of operation of the multiplier is first discussed in brief.

PRINCIPLE OF OPERATION OF THE MULTIPLIER UNIT

It has been shown that the input resistance of a grounded base junction transistor is given by[3]

$$r_{\text{in}} \doteqdot r_e + r_b(1-\alpha), \tag{1}$$

where r_e is the emitter resistance, r_b the base resistance, and α the short circuit current amplification factor. If a small alternating voltage v_e is fed to such a transistor stage from a low impedance source, then the output alternating current is given by

$$i_0 = \frac{\alpha v_e}{r_e + r_b(1-\alpha)}, \tag{2}$$

provided the output impedance is maintained at a low level. The emitter resistance r_e is related to the emitter bias current I_{in} as

$$r_e = \frac{kT}{qI_{\text{in}}} = \frac{1}{KI_{\text{in}}}, \tag{3}$$

where k=Boltzmann's constant, q=electronic charge, T=absolute temperature, and $K=q/kT$.

If $r_e \gg r_b(1-\alpha)$ then Eq. (2) reduces to

$$i_0 \doteqdot \frac{\alpha v_e}{r_e} = \alpha K v_e I_{\text{in}}. \tag{4}$$

Thus at constant temperature i_0 is proportional to the product of v_e and I_{in}.

For high I_{in} values $r_b(1-\alpha)$ is not negligible compared to r_e and the i_0-I_{in} relationship is no longer linear. The output then tends to fall below that expected from Eq. (4). A linear i_0-I_{in} relationship may be obtained over a reasonably good range of I_{in} values by introducing a compensating resistance R of correct value at the input as shown in Fig. 1.[2]

A single grounded base transistor compensated in the foregoing way cannot be used for constructing a four-quadrant multiplier because, as will be evident from Eq. (4), the arrangement will operate only with positive values of I_{in} and v_e. Operation with negative values of signals will be possible by maintaining finite quiescent values I_0 and v_0 of I_{in} and v_e, respectively. But for this case the output will no longer be given by Eq. (4). The new expression for output will also involve terms linear in I_{in} and v_e and these must be eliminated to get a true multiplier operation. To achieve this the entire plan of operation might be slightly modified in the manner shown in Fig. 2. Here two identical grounded base amplifier stages are used in cascade. The functions whose product is desired are converted into constant current sources X and Y and are added to the quiescent bias current in such a manner that the gain of one of these stages is controlled by X and that of the other by Y. The ac signal v_e now serves merely the purpose of a carrier. To achieve four-quadrant operation use has to be made of two such identical channels of operation, the signal inputs in one of which are 180° out of phase

[1] G. B. B. Chaplin and A. R. Owens, Proc. Inst. Elec. Engrs. (London), Monograph No. 2382 (July 1957).
[2] S. Deb and J. K. Sen, Electronic Eng. **31**, 753 (1959).
[3] R. F. Shea, *Principles of Transistor Circuits* (John Wiley & Sons, Inc., New York, 1954).

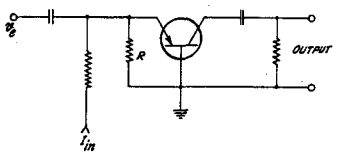

FIG. 1. The basic grounded base transistor amplifier for use as multiplier.

with those of the other. If the outputs of the two channels are combined in an adder stage one evidently gets a signal proportional to the product XY provided the gain and bias currents are such that the product $\alpha^2 I_0$ is the same for both the channels. Hence the entire multiplier unit should be as shown by the functional diagram in Fig. 3. A detailed description of the unit is given in the following.

THE MULTIPLIER CIRCUIT AND ITS OPERATION

In this section we describe a practical circuit diagram based on the principle as outlined. The phase shifting element as shown in Fig. 3, could be realized through the use of a grounded emitter transistor dc amplifier stage. Experience, however, showed that this introduces large thermal drift which cannot be satisfactorily eliminated by using a single NTC resistor at the input. Much better operation was obtained by using, instead of a phase shifting device, pnp transistors in one channel and npn in the other and feeding the same signal in both the channels. The emitter bias current of a pnp transistor is in the opposite direction to that of an npn one. Thus if the signal adds up to the bias of one it will be subtracted from that of the other. In one of the units tested the transistors used in the circuit were OC602 (pnp) and 2N356(npn). The compensating resistance R as found by experimentation was 1kΩ for OC602 and 4.7 kΩ for 2N356 transistors.[2] In the absence of signals the rf outputs were made equal by adjusting the bias. When a signal was present in any one of the amplifier stages the rf voltage output appeared as a modulated wave. The depths of modulation for both X and Y amplifiers in the two channels were made equal for the same signal input by adjusting the values of the resistances which converted the signal voltages to proportional currents. A constant voltage feed to the second stage of a channel was ensured by the requirement of small output impedance of the first. The precise details of the interstage network are dictated by the requirement of filtering the signal from the modulated carrier at the output of the first stage. The simplest way in which this can be done consists in using either a C-R filter or a series tuned circuit. But with low frequency transistors, both for adequate bandwidth and low phase shift required to ensure that the variables X and Y in a given channel are impressed upon the carrier before

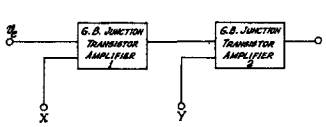

FIG. 2. The modification of the basic multiplier for four-quadrant operation.

undergoing any relative displacement in phase, none of these devices would be quite ideal. As a compromise a series tuned circuit with low Q value was used. It is to be noted that the problem of bandwidth becomes easier if the carrier frequency is chosen high. This in turn requires the use of a transistor with a high value of cutoff frequency. In another unit tested use was, therefore, made of OC612 transistors in the place of OC602 in the pnp channel. The filters at the end of the transistor amplifiers in both the channels were of course of the C-R type. These, however, introduced identical phase shifts in the two channels and as such did not affect the operation. The details of a circuit incorporating these features are shown in Fig. 4. Simple resistance adders were used and these were followed by an amplifier and detector of the conventional type. It may be pointed out that with a unipolar detector the output also contains a dc component corresponding to the unmodulated carrier. An auxiliary adder stage after the detector was, therefore, used to balance out this dc component. Proper setting of initial condition of the subsequent operational amplifier of the computer would also enable one to balance out this component.

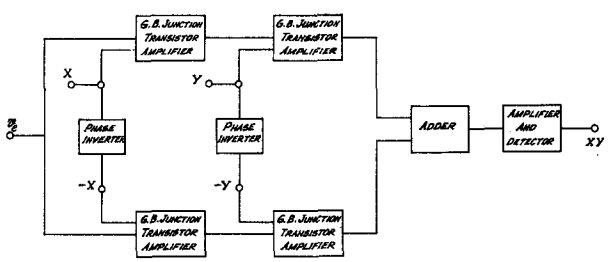

FIG. 3. Schematic diagram of the four-quadrant transistorized multiplier.

TEST RESULTS AND THE PERFORMANCE OF THE MULTIPLIER

Some experimental results obtained with the multiplier shown in Fig. 4, will now be described. The multiplier characteristics with OC602 transistors in the pnp channel and a carrier frequency of 100 kc are shown in Fig. 5(a) for a fixed value of X, viz., ±7.5 v, and various values of Y. The reciprocal characteristics with a fixed value of Y, viz., ±7.5 v and various values of X are given in Fig. 5(b). Characteristics are evidently quite satisfactory. Deviations from strict linearity occur both at very low and high values of input signals. The fractional error at low inputs is dependant upon the extent of carrier elimination and this will be presently discussed. For 10-v input signals the deviation from linearity is within 3% for both the variables X and Y. The operation was found to be flat over a bandwidth of 3 kc. This figure of course does not compare favorably with those reported for other types of multiplier. But the performance in this respect could be considerably improved by using different types of transistors. Thus, in

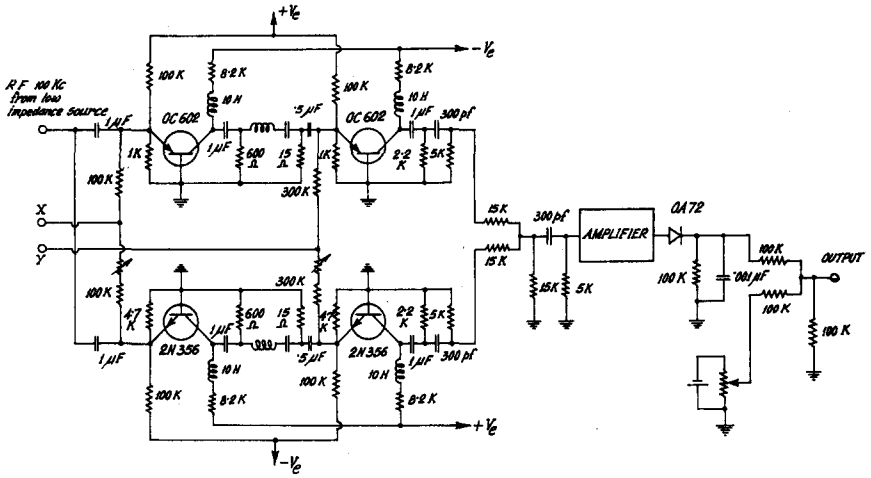

FIG. 4. Circuit diagram of the four-quadrant transistorized analog multiplier.

the other unit previously mentioned, the use of an OC612 transistor in place of the OC602 permitted one to increase the carrier frequency to 500 kc. For this unit the response was found to be flat over a 15-kc frequency band. It is to be noted that in all these observations the limits of the bandwidth were taken to be the points at which the response fell by 5% of the midband value. If the limits are taken to be the 3-db points, as is the current engineering practice, the figures would be increased. Thus, the 3-db bandwidth was 4 kc for the unit using the OC602 transistor and 20 kc for that using the OC612. This latter value compares favorably with the values achieved in other types of multipliers.[4,5] For example, for the crossed field type a value of 10 kc can rarely be exceeded. Devices using the square-law characteristics of germanium diode and square wave generator give a comparable value. Only some of the beam deflection type of multipliers are potentially capable of achieving or even exceeding such a value. But the formation and maintenance of a uniform beam is quite a difficult problem with such multipliers. It is of course to be remembered that transistors having a frequency response much better than any of the discussed types are also available and a bandwidth much higher than 20 kc may be achieved by using such transistors.

Regarding temperature effect, good stability could be obtained for the circuit shown in Fig. 4 by using negative temperature coefficient resistors in the manner already discussed.[2] In the present circuit both the operational stages were almost equally vulnerable to the effect of temperature. The stability of the individual stages could be maintained within 1–2% by the afore-mentioned resistors. With identical channel characteristics the residual drift on this account affected mainly the contribution due to the carrier as discussed later. Operation extending over 6 hr also showed that the long time drift was roughly 3%.

[4] C. L. Johnson, *Analog Computer Technique* (McGraw-Hill Book Company, Inc., New York, 1956).
[5] L. Marton, editor, *Advances in Electronics and Electron Physics* (Academic Press, Inc., New York, 1955).

It may be noted that in contrast to the familiar balanced modulator operation the suggested arrangement (Fig. 3) gives an output which contains the contributions due to the carrier. This can, however, be eliminated to any desired degree by the methods already mentioned. In the present case through careful adjustment the contribution due to the carrier could be kept within 0.05 mv. The limit to carrier elimination is evidently set by the precision and stability of the potential dividing resistors. A more pertinent problem related to the present circuit is the possible leakage of the individual signal components X and Y at the output. Thus, with $X=Y=400$ cps the product term is represented by the 800-cps component. Nevertheless, owing to the lack of perfect symmetry of the multiplier channels the 400-cps term might also appear at the output. The magnitude of the latter relative to the 800-cps term can be estimated by measuring the strengths of the fundamental and the second harmonic with the help of a wave analyser. Such a measurement showed that the fundamental was at least 40 db below the second harmonic. This could undoubtedly be improved further by careful design of the amplifier channels. Proper selection of transistors and their operating points and of the adder resistances are essential for this purpose. As regards transistors the gain and the bias conditions of the units in a given channel must be the same and the product $\alpha^2 I_0$ must be the same for both the channels. Regarding the adder resistances, these must be as nearly identical as possible. In the present case the equality, as found by actual measurement, was not much better than 1%, a figure which would easily account for a substantial part of the observed leakage signal at the output. Careful adjustments of the amplifier channels and a more accurate choice of these resistors should reduce the leakage considerably and a 60-db suppression of the individual signal component should be easily realizable at low levels.

Apart from the fundamental, harmonics higher than the second might also appear at the output owing to the presence of distortion. It had been shown that for a single stage

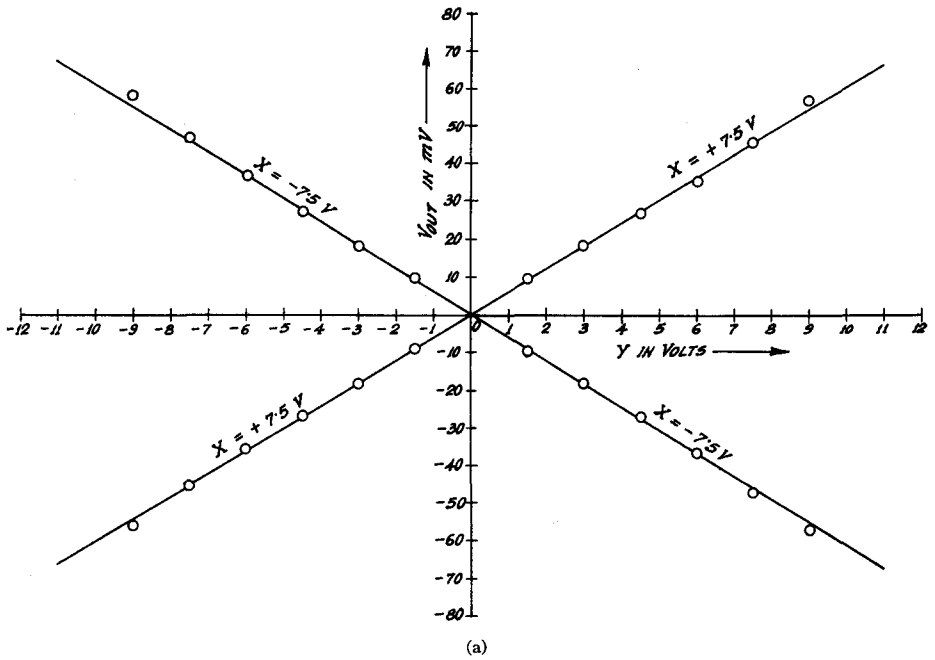

FIG. 5. (a) and (b). Multiplier characteristics of the circuit shown in Fig. 4.

multiplier the distortion was indeed very small—certainly below 5%.[2] In the present case too, measurement with a wave analyser revealed that all higher harmonic terms apart from the third were negligible. Nonetheless, even this third harmonic term was at least 40 db below the second.

Investigations also showed that there was no detectable nonlinearity or hysteresis of the characteristics near the origin, the minimum detectable signal with the present measuring setup being 0.05 mv.

ACKNOWLEDGMENT

Thanks are due Professor S. K. Mitra and Professor J. N. Bhar for their kind interest in the work and to Dr. A. K. Choudhury for helpful discussions.