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Revisiting the role of trap-assisted-tunneling process on current-voltage characteristics in tunnel field-effect transistors

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This paper discusses the role of trap-assisted-tunneling process in controlling the ON- and OFF-state current levels and its impacts on the current-voltage characteristics of a tunnel field-effect transistor. Significant impacts of high-density traps in the source region are observed that are discussed in detail. With regard to recent studies on isoelectronic traps, it has been discovered that deep level density must be minimized to suppress the OFF-state leakage current, as is well known, whereas shallow levels can be utilized to control the ON-state current level. A possible mechanism is discussed based on simulation results. *Published by AIP Publishing*. https://doi.org/10.1063/1.5010036

I. INTRODUCTION

A silicon-on-insulator (SOI) "lubistor (Lateral, Unidirectional, Bipolar-type Insulated-gate TransiSTOR)" having a single p-n junction was proposed for high-current applications in 1982,[1,2] which has already been applied to electrostatic discharge (ESD) protection circuits.[3] Band-to-band tunneling (BTBT) and negative differential conductance across the forward-biased p-n junction of a SOI lubistor are observed.[4] Several articles discussing the negative differential conductance have already been published,[4–8] and the fundamental mechanisms of negative differential conductance of Si-based SOI lubistors have been analyzed successfully.[7,8] Recently, several discussions on the reverse-biased tunnel current characteristics of the SOI lubistor [so-called "tunnel field-effect transistor" (TFET)] at room temperature focusing on low-standby power device applications and fast switching have been made in the literature,[9–15] where three-dimensional (3-D) transport was assumed.

In recent years, impacts of tunnel dimensionality on the tunnel field-effect transistor (TFET) performance are also studied and discussed from the viewpoint of drivability of TFET.[16–20] Ultrathin SOI lubistors reveal two-dimensional (2-D) transport and 2-D tunnel behavior,[8,21] which were clearly demonstrated at low temperature. In addition, it has been demonstrated experimentally that the carrier-transport dimensionality in the reverse-biased ultra-thin SOI lubistor (TFET operation mode) significantly alters nature of the reverse-biased current behavior even at room temperature.[21] Also, the two-dimensional quantum confinement of the system made deep trap levels of the device effectively shallower.[21,22] The carrier confinement effect on the generation-recombination process also attracts attention in understanding the low-dimensional carrier injection mechanism in ultrathin SOI devices;[22] this phenomenon is important particularly for the lateral bipolar transistor on the ultra-thin silicon-on-insulator substrate.[23,24]

However, some behaviors including low-temperature transport characteristics of the tunnel FET have not yet been well elucidated. Although Tabe recently addressed the transport characteristics of the atomic layer p-n junction on an insulator film,[25] the behavior of the device does not cover the physics of ultra-thin SOI tunnel FET because the device did not have the MOS gate that strongly confines carriers. As the impact of low dimensionality of the tunnel process on the performance of SOI tunnel FET has not been completely analyzed either experimentally or theoretically, we must elucidate the transport physics to advance the performance of SOI tunnel FET. Although the availability of isoelectronic traps for the enhancement of TFET drivability has recently been discussed,[26,27] it is controversial because the mechanism assumed is not simple as expected.

This paper theoretically discusses different aspects of experimental results conducted on ultra-thin SOI tunnel FET (reverse-biased ultra-thin SOI lubistor) at low temperature (down to 35 K) to evaluate the impact of trap-assisted tunneling (TAT) on the tunnel characteristics and generation-recombination process. The influence of bulk traps (both deep levels and shallow levels) in the tunnel region inside the source on the subthreshold behavior and ON-current characteristics of the device is investigated with the aid of device simulations. In the consideration, the impact of the quantum confinement of carriers on the trap-assisted tunneling is discussed based on the theoretical point of view. Finally, it is also discussed comprehensively how we can control the performance of the ultra-thin SOI tunnel FET.

II. DEVICE STRUCTURE AND SIMULATIONS

A. Device structure and measurements

In this paper, SOI lubistors[1] with a lateral p^+-p-n^+ structure, fabricated on a (001) silicon-on-insulator substrate with a 110-nm buried oxide layer, is used in experimental characterizations;[7,21] the lateral p^+-p-n^+ structure lies along the ⟨100⟩ direction. The device has a 5-nm-thick gate oxide layer and a 10-nm-thick Si layer; the schematic device structure is shown in Fig. 1(a). The n^+-Poly-Si gate is 3-μm long and 10-μm wide. Doping concentrations of the p^+ source, channel, and n^+ drain are 4×10^{20} cm^{-3}, $\sim 1 \times 10^{16}$ cm^{-3},

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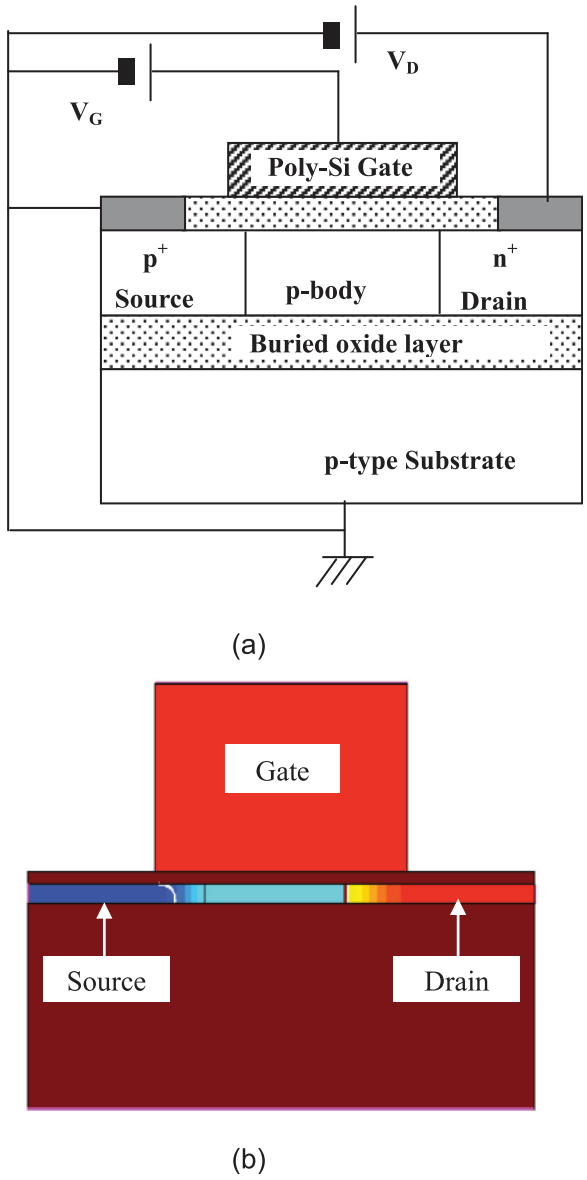

FIG. 1. Schematic device structure of the lubistor. The bias configuration is the same as that for n-type tunnel FETs. (a) Device structure fabricated on the silicon-on-insulator (SOI) wafer and (b) device structure used for device simulations.

and 4×10^{20} cm^{-3}, respectively. The phosphorus doping concentration of the n^+ poly-Si gate is 4×10^{20} cm^{-3}. These parameters are summarized in Table I. The gate-source overlap length and the gate-drain overlap length are both 40 nm; it is anticipated that the vertical tunneling in the gate-source overlap region and the gate-drain overlap region may occur.[28,29] The source electrode (the anode electrode of the lubistor) is grounded and drain electrode (the cathode electrode of the lubistor) is positively biased ($0\,V < V_D < 1\,V$) for the reverse-biased condition of the source junction. The gate electrode is always positively biased ($0\,V < V_G < 3.5\,V$). Since the gate oxide is slightly thick, the gate voltage is slightly high; its value can be reduced to sub-1-V by using a thin high-k oxide layer like HfO_2. Therefore, the gate voltage range in this experiment is acceptable for modern sub-1-V operation. Possible device dimensions for the sub-1-V operation are discussed, and device simulation results are demonstrated later. The device characteristics are evaluated at low temperature down to 35 K.

In this experiment, no negative bias was applied to the gate electrode. When the positive gate bias induces an inversion layer (electrons) beneath the gate oxide layer, the confinement of electrons is controlled by the thin silicon layer. This means that a more significant 2-D confinement effect appears in the inversion layer. This is the reason why the positive gate bias is used.

In contrast to Refs. 26 and 27, no intentional doping of impurity atoms is made to introduce specific trap levels, such as isoelectronic traps in the channel region. It is expected that vertical tunnel takes place around the gate-overlapped source junction region. I_D-V_G and I_D-V_D characteristics were measured from 35 K to 250 K.

B. Simulations

We performed various device simulations in order to reproduce I-V characteristics of the fabricated device. Device parameters assumed here are summarized in Table I. For simulations, we assume the Hurkx non-local tunnel model associated with the trap-assisted tunneling (TAT) model[30] in the Sentaurus device simulator.[31] We assume two-different trap levels (0.085 mV and 0.3 eV). The trap level of 0.085 eV

TABLE I. Device parameters of the fabricated device and those for simulations. Boldface parameters play important roles in the discussion.

	Values (units)		
Parameters	Fabricated device	Simulations	Simulations (scaled device)
Gate length (L_G)	3 (μm)	200 (nm)	200 (nm)
Gate oxide thickness (T_{ox})	5 (nm)(SiO_2)	5 (nm) (SiO_2)	3 (nm) (HfO_2, EOT = 0.5 nm)
Silicon layer thickness (T_{si})	**10 (nm)**	**10 (nm)**	**10 (nm)**
Buried oxide thickness	**110 (nm)**	**110 (nm)**	**110 (nm)**
Body doping (N_B)	10^{16} (cm^{-3})	10^{16} (cm^{-3})	10^{16} (cm^{-3})
Source doping (N_S)	4×10^{20} (cm^{-3})	4×10^{20} (cm^{-3})	4×10^{20} (cm^{-3})
Drain doping (N_D)	4×10^{20} (cm^{-3})	4×10^{20} (cm^{-3})	4×10^{20} (cm^{-3})
Gate-Source overlap length	**40 (nm)**	**40 (nm)**	**40 (nm)**
Gate-Drain overlap length	**40 (nm)**	**40 (nm)**	**40 (nm)**
Trap concentration	...	**10^{16}–10^{20} (cm^{-3})**	**10^{16}–10^{20} (cm^{-3})**
Trap levels	**0.085, 0.13 eV**	**0.085, 0.30 eV**	**0.085 eV**
Gate electrode	**n+ poly-Si**	**n+ poly-Si**	**n+ poly-Si**

is extracted from the experimental results,[21] while that of 0.3 eV is assumed as a deep level. In simulations, we assume that trap levels exist only in the p-type source region. We assumed a high density of traps for the device in simulations because it was anticipated that the source region has a high density of traps due to the ion-implantation-oriented defects. In addition, we also performed the simulation at 400 K. This temperature condition and the trap density are so chosen as to enhance their impact on I_D-V_G characteristics.

III. RESULTS AND DISCUSSION

A. Preliminary results obtained by simulations

Figure 2 shows two simulation results assuming two different trap energy levels (0.085 eV and 0.3 eV) at 400 K, where traps are assumed only inside the source. The energy level of 0.085 eV represents a shallow trap level obtained by experiments shown later (see Fig. 7).[21] The energy level of 0.3 eV is assumed as a deep trap level in this study. It is observed that shallow trap levels do not significantly alter the OFF state characteristic although the OFF-current level is slightly increased. In contrast, deep trap levels drastically increase the OFF current level.

In order to discuss the impact of different energy levels of traps on the I-V characteristic of the device, we show schematic images of carrier transport based on the energy band diagram in Fig. 3; Fig. 3(a) shows schematic energy-band diagrams for the TFET with deep traps, and Fig. 3(b) shows schematic energy-band diagrams for the TFET with shallow traps. "x" represents the trap level and arrows suggest possible transition processes of electrons. Both figures also show the energy band diagrams in both the ON-state and OFF-state of the device.

We can see the definite difference between the device with deep levels and shallow levels. In the OFF-state, the

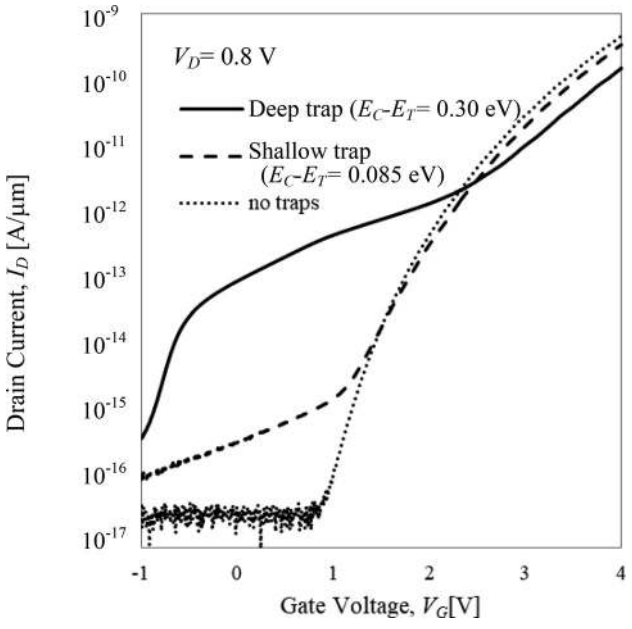

FIG. 2. I_D-V_G characteristics including the TAT current for two different trap levels at 400 K (simulations). It is assumed that the local density of traps (N_T) is 10^{20} cm^{-3}.

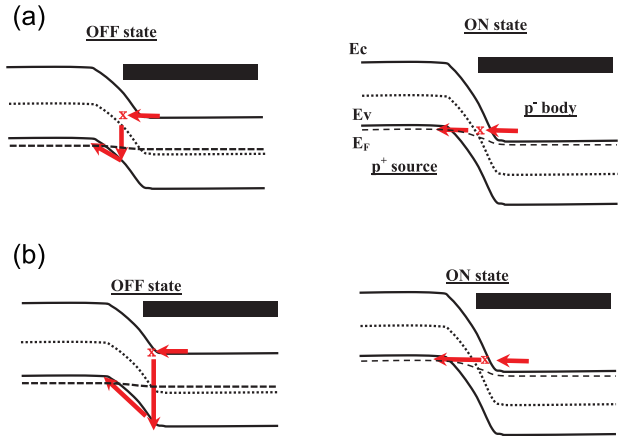

FIG. 3. Impacts of different energy levels of traps on the trap-assisted tunneling. (a) Device with deep levels and (b) device with shallow levels.

trap-assisted tunneling process is shown in Figs. 3(a) and 3(b) for deep and shallow trap levels, respectively. In the case of the deep level, the electron in the conduction band of the channel region tunnels to the trap site, and it might lose own energy so as to recombine with a hole in the valence band. This recombination process takes place easily because the hole density in the valence band is sufficiently high due to the proximity of the recombination location to the source region. In the case of the shallow level, however, the recombination location is far from the source region where the hole density in the valence band is very low, which interferes the recombination process of electrons. Therefore, the leakage current level in the OFF-state is low for the TFET with shallow trap levels. This is illustrated in Fig. 3(b).

On the other hand, the TAT process shown in Fig. 3(a) in the ON-state is very similar to that in Fig. 3(b). The difference seen in Figs. 3(a) and 3(b) in the ON-state simply seems to be the tunnel probability of electrons. However, the background phenomenon is not so simple because the ON-state current level of the TFET with deep trap levels is lower than that with shallow trap levels. The possible reason for this is discussed in Subsection III B.

B. Influence of trap levels of the source region on the ON-current characteristics

As shown in Fig. 2, the ON-state drivability of the device with deep level traps is less than that with shallow level traps. The energy band diagram of the device in the OFF-state is shown in Fig. 4(a). It is observed in Fig. 4(a) that the energy band diagram of the device with deep level traps is almost the same as that with shallow level traps. However, the OFF-state current level depends on the energy level of traps as shown in Fig. 2. The energy band diagram in the ON-state for devices with both deep-level traps and shallow-level traps is shown in Fig. 4(b). It is observed in Fig. 4(b) that the electrostatic potential of the body region adjacent to the source region is affected by the trap levels of the source region (see a circle near the source). The upward potential shift of the energy band is almost equal to $E_c - E_t$, where E_t is the trap level. It is anticipated that traps in the source pin the Fermi level and then they deplete electrons of

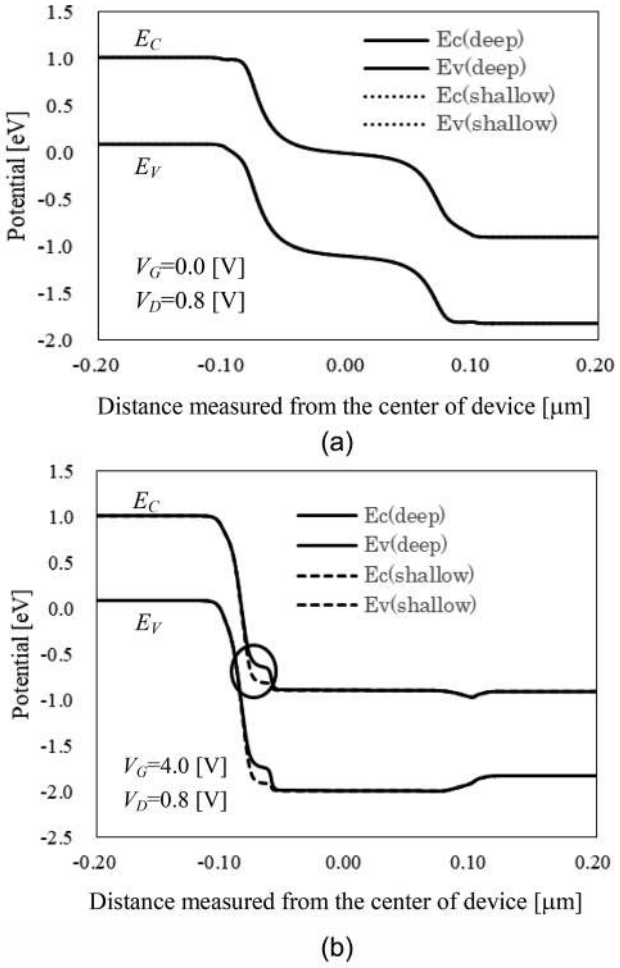

FIG. 4. Energy band diagrams of TFETs with shallow and deep trap levels for three-different gate voltage conditions. The device parameters shown in Table I are used. (a) OFF state and (b) ON state.

the channel region that are induced by the gate electrode. This situation is shown again in Fig. 5, where "x" denotes the trap level. Although the channel region is fully covered by the gate electrode, it is anticipated that the impact of the Fermi-level pinning is stronger than the gate-induced electric field near the source region. The upward electrostatic potential shift interferes the electron tunneling from the channel region to the source because the tunneling distance increases as seen in Figs. 4 and 5. Due to such a potential shift of the TFET with deep-level traps, the ON-current level of the TFET with deep-level traps is lower than that with shallow-level traps as seen in Fig. 2.

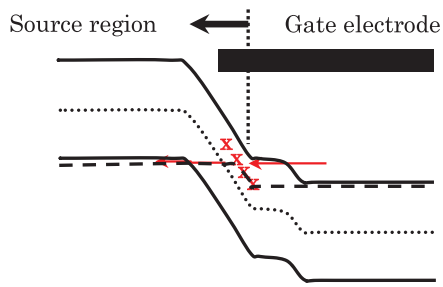

FIG. 5. Energy-band diagram and electron transport in the ON state.

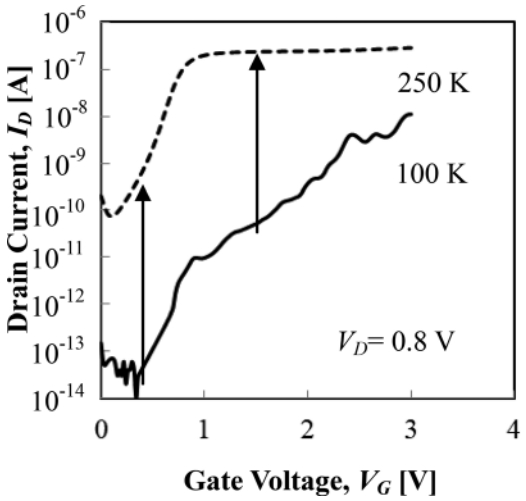

FIG. 6. I_D-V_G characteristics for two different temperatures at $V_D = 0.8$ V.

C. Experimental results and their aspects

Experimental I_D-V_G characteristics, obtained at 100 and 250 K, are shown in Fig. 6. It is observed in Fig. 6 that the OFF-state leakage current level at V_G of 0.5 V and the ON-state current level at V_G of 1.5 V are both sensitive to temperature. However, the temperature dependence of ON-state current is somewhat less at a high V_G value. This is due to the fact that the TAT process, which is more sensitive to temperature, dominates at low V_G values, whereas the BTBT process, which is relatively less temperature sensitive, dominates at high V_G values.

We measured the drain current at various temperatures in order to elucidate the influence of traps on I_D-V_G characteristics in the OFF state (@$V_G = 0.5$ V) and ON state (@$V_G = 1.5$ V). Arrhenius plots shown in Fig. 7 yield two different trap levels (85 meV and 130 meV).[21] It is found that deep-level traps rule the OFF-state current behavior and shallow-level traps rule the ON-state current behavior. As a result, the deep-level-trap density increases the OFF-state leakage current whereas shallow levels influence the ON-state current level. Since no intentional doping to introduce specific traps, such as isoelectronic traps,[26,27] is performed in the

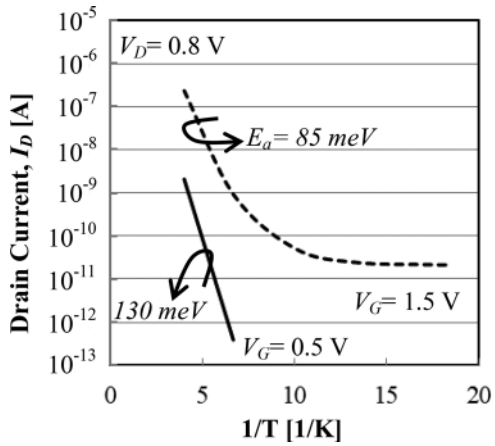

FIG. 7. Arrhenius plot of drain current at $V_D = 0.8$ V and at $V_G = 0.5$ V and 1.5 V. E_a is the activation energy in units of eV.

device, it is anticipated that the phenomena observed here are different from those demonstrated in Refs. 26 and 27. It is worth noting that deep-level traps do not impact the ON-state current level directly. It is suggested in Refs. 21 and 22 that quantum confinement of carriers apparently makes energy levels of traps shallower than their original levels. The consideration described in Refs. 21 and 22 is supported by the demonstration of the high performance bipolar transistor in Ref. 23. It is also expected that the new finding in this study should be useful in understanding and, hence, improving the drivability of thin-semiconductor-layer-based tunnel FETs.

Finally, the temperature dependence of subthreshold swing (*SS*) of the device is shown in Fig. 8. *SS* holds a very small value for $T < 100\,K$. The temperature dependence of the *SS* value shows that "100 K" seems to be a critical temperature, which suggests that the TAT current via deep-level traps becomes dominant for $T > 70\,K$. Figures 2 and 6–8 strongly suggest that reduction of the density of deep-level traps should improve the *SS* value at room temperature.

D. Performance prediction of scaled vertical TFETs by simulations

We examined the TFET performance with scaled dimensions. The device parameters assumed for the simulation are also shown in Table I. Here, the device is assumed to have only shallow-level traps ($E_a = 0.085\,eV$, $N_T = 10^{20}\,cm^{-3}$) in the source region. Simulated I_D-V_G characteristics for two different values of V_D, as 0.8 V and 0.1 V, are shown in Figs. 9(a) and 9(b) for the devices with and without shallow-level traps in the source region, respectively.

The threshold voltage obtained by the normalized conductance method[32] is 0.55 V at $V_D = 0.8\,V$ regardless of shallow-level traps and the drain current is $2 \times 10^{-8}\,A/\mu m$ at $V_G = 1.0\,V$ and $V_D = 0.8\,V$. The subthreshold swing (SS) value is 38 mV/dec without any traps and 61 mV/dec with shallow-level traps of $10^{20}\,cm^{-3}$ at $V_D = 0.8\,V$. These performance parameters are very good except the drain current level and the OFF-state leakage current level. The OFF-state leakage current is very high even at $V_D = 0.1\,V$. Since the present leakage current level should be reduced by 4 orders from the point of view of the suppression of standby leakage current,

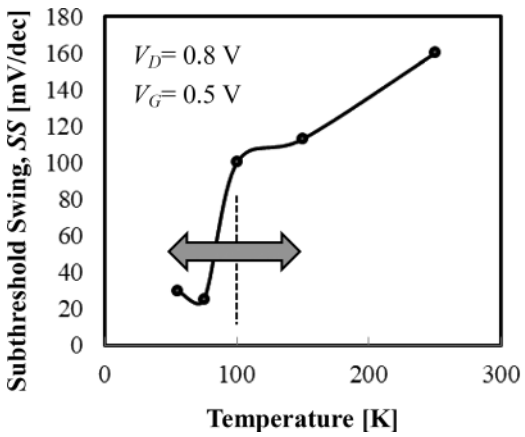

FIG. 8. Plot showing the temperature dependence of subthreshold swing.

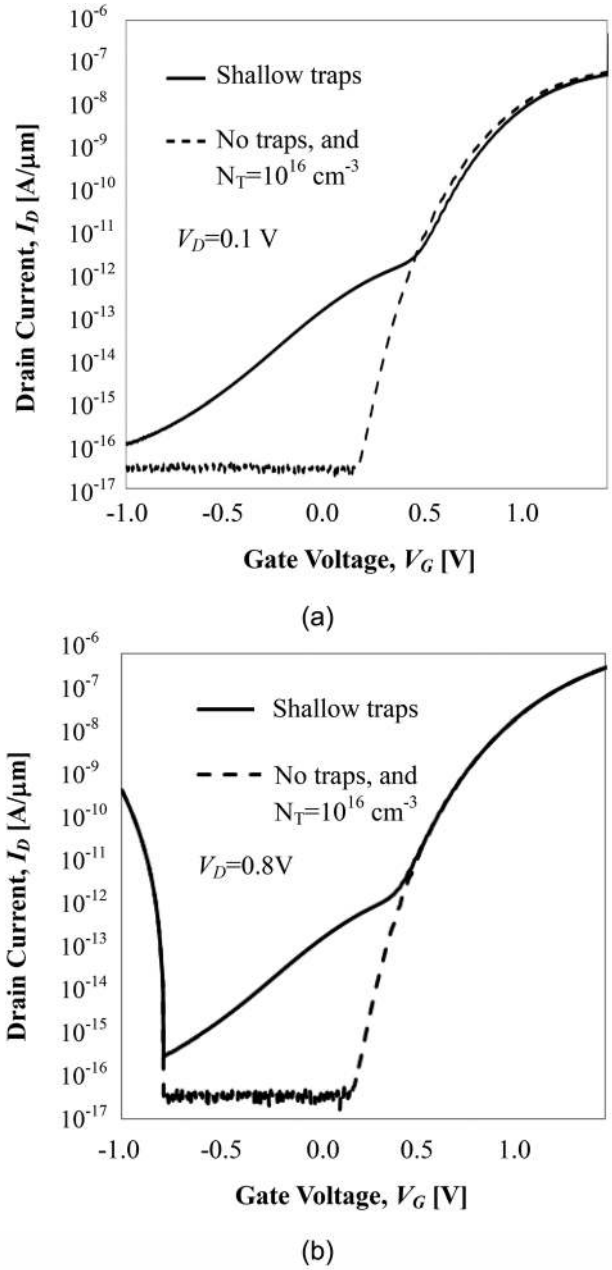

FIG. 9. Simulation result of I_D *vs.* V_G characteristics for scaled vertical TFET. The impact of shallow-level traps in the source diffusion is compared. Solid line id for $N_T = 10^{20}\,cm^{-3}$ and broken line for $N_T = 10^{16}\,cm^{-3}$ and $N_T = 0\,cm^{-3}$. (a) $V_D = 0.1\,V$ and (b) $V_D = 0.8\,V$.

the trap density must be roughly reduced to $10^{16}\,cm^{-3}$ as shown in Fig. 9. Ambipolar current is also observed in Fig. 9(b) for $V_D = 0.8\,V$ and negative gate bias, which is due to BTBT at the drain junction. Such ambipolar current can be eliminated by lowering the doping level of the drain or using underlap gate-drain architecture. The drain current level can be improved by using germanium or compound materials.

IV. CONCLUSION

This paper discussed the impacts of shallow-level traps and deep-level traps in the source region of tunnel field-effect transistors, which are fabricated in a thin silicon layer

on the silicon oxide layer, on tunnel current characteristics. The following points are elucidated.

(1) Simulation results have demonstrated that deep-level traps drastically increase the OFF-state leakage current as expected but that shallow-level traps do not increase the leakage current so much despite its density is so high.
(2) Simulation results have demonstrated that high-density traps in the source diffusion pin the Fermi level of the channel region, which results in the decrease in the ON-state tunnel current. However, this negative impact due to shallow-level traps is very limited. This influence is suppressed by reducing the shallow trap density.
(3) Experimental results supported that deep-level traps in the source region significantly degrade the subthreshold swing value. However, the ON-state tunnel current level is influenced only by shallow-level traps, which is expected by the Fermi-level pinning due to the high trap density in the source region.
(4) It has been demonstrated both by simulation and experiment that the density of deep-level traps in the source diffusion should be reduced in order to suppress the OFF-state leakage current and to sharpen the subthreshold swing. In addition, it has been demonstrated that shallow-level traps in the source region play an important role in controlling the ON-state tunnel current.
(5) Simulation result of scaled device demonstrated better performance of TFET except the drain current level and the OFF-state leakage current level. The OFF-state leakage current level can be lowered by reducing the trap density and the ON-current level can be improved by using germanium or compound materials.

ACKNOWLEDGMENTS

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