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# Luminescence and deep-level characteristics of GaAs/Si with atomic layer epitaxy grown predeposition layers

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A relatively simple scheme for the growth of high optical quality GaAs layers on Si substrates by metalorganic chemical vapor deposition (MOCVD) technique is reported. The process is analogous to the conventional two-step growth procedure where the initial thin nucleating layer growth is done by atomic layer epitaxy (ALE) technique, implemented into the MOCVD reactor itself. The photoluminescence from the layer is increased to about sixfold by replacing the normal predeposition growth by the proposed ALE growth technique. Magnitude of luminescence is comparable to that obtained from layers grown with strained layer superlattice buffers. A number of electron and hole traps are detected in the material by deep-level transient spectroscopy and photocapacitance experiments. A particular electron trap with an activation energy of 0.76 eV is identified as the main nonradiative center by virtue of the decrease of its density in the same proportion as that of the increase in luminescence intensity. Density of some other electron traps are also reduced as a consequence of ALE predeposition. © *1996 American Institute of Physics.* [S0021-8979(96)02010-5]

## I. INTRODUCTION

Two major techniques, namely, III-V semiconductor growth on Si and III-V semiconductor wafers attached to Si substrates by Van Der Waals force, have been used to combine the beneficial properties of Si with that of III-V compounds. Of these, growth of GaAs on Si has been studied most for applications in high-speed microwave devices and optoelectronic integrated circuits.[1] However, the most important challenge to be met towards achieving this goal is to obtain GaAs layers on Si with quality comparable to that of bulk GaAs materials. The large lattice mismatch of the GaAs layer with the Si substrate and the difference in thermal expansion coefficients of the two semiconductors, give rise to a large density of misfit dislocations at the interface. A major part of these dislocations thread into the epitaxial layer, making the latter unsuitable for any device application. The growth of a polar semiconductor GaAs on nonpolar Si also presents some serious difficulties. Absence of any predetermined bonding sites for cations and anions in the initial stages of growth, results in the formation of antiphase domains (APD) due to As–As and Ga–Ga bonds.[2] These APDs are electrically active and they make the epitaxial layer behave like a highly compensated semiconductor. The devices fabricated on such layers show relatively poor performance. To reduce the problem of GaAs layer degradation, a two-step growth procedure[3] has been introduced where an initial low-temperature nucleation layer growth is followed by the usual high-temperature growth. Insertion of a strained layer superlattice (SLS) between the layer and the substrate has been found to be quite effective in removing the threading dislocations laterally along the interface.[4] Several other variations of the growth procedure or post-growth processing have been used to minimize the problem of thermal stress and dislocations.[5–9] Further, use of slightly misoriented substrates is commonly made to lower the density of APDs.[10] It has been found that a two-dimensional (2D) growth, compared to a three-dimensional growth, forms reduced density of APDs.[11] Kitahara *et al.*[12] have shown that the use of atomic layer epitaxy (ALE) at the initial stages of GaAs growth on Si, results in a two-dimensional growth at a comparatively early stage of growth. We have used this information to develop a simple two-step growth procedure for GaAs/Si where the initial low-temperature growth of a thin nucleation layer is done by ALE, favoring the formation of a lower density of APDs. In order to check the quality of the layers, grown by this technique, we have characterized them using photoluminescence (PL), deep-level transient spectroscopy (DLTS), and photocapacitance. Similar experiments were performed on GaAs/Si materials grown under similar conditions by conventional two-step techniques with or without SLS interfacial buffers. Properties of these three kinds of materials have been compared to show the usefulness of our technique. The details of the work are being presented here.

## II. MATERIALS GROWTH

The growth of GaAs/Si layers was done in an atmospheric pressure metalorganic chemical vapor deposition (MOCVD) system. The substrates were $2\times1$ cm$^2$ *n*-type (100) Si ($>1\times10^{18}$ cm$^{-3}$), 3° off towards <110>. Substrate cleaning was done by the usual degreasing in organic solvents, followed by oxide removal in buffered HF. Finally, the surface of the Si substrate was hydrogen terminated using a 1HF+1$H_2O$ dip followed by spin drying in flowing nitrogen. The wafers were then loaded into the MOCVD reactor and baked under arsine/hydrogen ambient at 970 °C for 5 min to desorb the residual impurities.

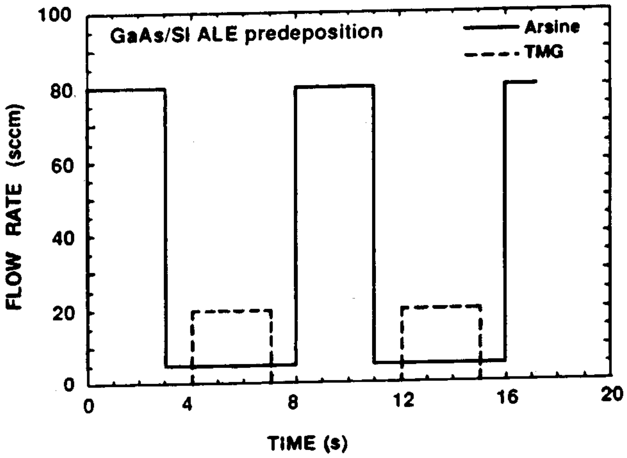


FIG. 1. Flow modulation scheme for ALE growth of predeposition layer in GaAs/Si.

Three types of samples were grown in the MOCVD reactor. The first (sample No. I) was grown by a conventional two-step process. The predeposition layers for nucleation consisted of a 20-nm-thick GaAs, grown at 425 °C, which was then annealed at 725 °C for 10 min. The final GaAs layer was 2 $\mu$m thick, grown at 650 °C at the rate of 1.5 $\mu$m/h. The second (sample No. II) was grown in a similar fashion. However, in this case, a (2 nm) $GaAs_{0.91}P_{0.09}$/(2 nm) GaAs SLS with ten periods was grown at 650 °C and inserted between the predeposited and the final GaAs layers. The thickness of the ternary component was within the critical value and the strain component was kept low in order to avoid a rough surface.[13] Finally, the third (sample No. III) was grown by our proposed technique where the predeposition layer consisted of a 20-nm-thick GaAs layer, grown at 425 °C using ALE. This was followed by the usual 2 $\mu$m GaAs growth at 650 °C. The ALE growth procedure was implemented in the MOCVD reactor itself. The Ga and As sources were switched alternatively for the periods of 3 s each with 1 s intervals. The As flow rate was switched between 80 and 5 sccm. The flow rates of trimethylgallium (TMG) and arsine ($AsH_3$) were properly controlled to obtain a growth rate of 400 nm/h for GaAs growth on GaAs. The flow modulation scheme is shown schematically in Fig. 1. The ALE growth procedure, so implemented, is quite simple as the layer was thin and it did not require any layer to layer control over the composition and thickness as in the case of SLS growth. The surface of the final layer, grown by usual MOCVD technique over the ALE-grown nucleation layer was mirror smooth, as observed under a Nomarski Interference Contrast Microscope. The surface of sample II, containing SLS buffer, on the other hand, showed faint cross-hatchet patterns indicating generation of additional dislocations at the GaAs/SLS interface.

## III. CHARACTERIZATION

The background carrier concentrations of all our GaAs/Si layers were around $10^{17}$ $cm^{-3}$, $n$-type. However, the same value for the layers, grown under similar conditions on GaAs substrates, was about $10^{15}$ $cm^{-3}$. The observed higher value of carrier concentration in GaAs/Si is usual and is attributed to autodoping of the epitaxial material by the Si substrate.[13] This effect is usually minimized by increasing the layer thickness.

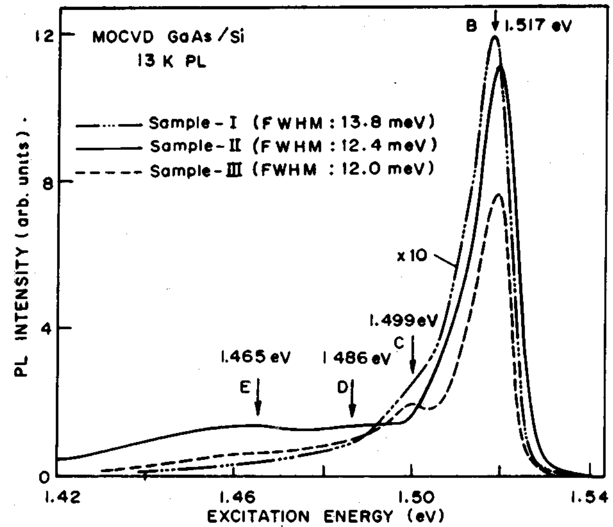


FIG. 2. PL spectra for GaAs/Si samples grown under three different conditions.

Luminescence efficiency of each layer was characterized by PL measurements at 13 K. Optical excitation was obtained at 0.4 $kW/cm^2$ of the 514.5 nm line of an Argon ion laser. Luminescence spectra were resolved with a 0.64 m spectrometer and detected in a S1 photomultiplier.

DLTS measurements were done on the layers in the temperature range of 100—350 K to resolve the electron traps present in the same. An evaporated gold (0.5 mm diameter) Schottky barrier diode was fabricated on the layer surface to facilitate the experiment. Description of our DLTS setup was presented elsewhere.[14]

Steady-state photocapacitance measurements were done at 20 K on the same test devices used for DLTS measurements. The purpose of this experiment was to support and to complement the results obtained from DLTS experiments. The photocapacitance scan in our experiment was limited to the incident photon energy range of 0.62—1.26 eV and hence only those traps having photoionization energies within this limit were detected. The details of our photocapacitance experiment and the setup used was given in a previous publication.[15]

## IV. RESULTS AND DISCUSSIONS

### A. PL

The 13 K PL spectra for samples I, II, and III are shown in Fig. 2. The major luminescence from all samples is due to peak ''B'' situated at ~1.5163 eV and is attributed to conduction band to carbon acceptor and donor to carbon acceptor transitions. The height of this peak is considerably larger at ten and six times, respectively, for samples II and III, compared to that for sample I. High PL intensity is a direct indication of reduced defect density and impurities in the material.[16] We can thus say that, like the incorporation of a

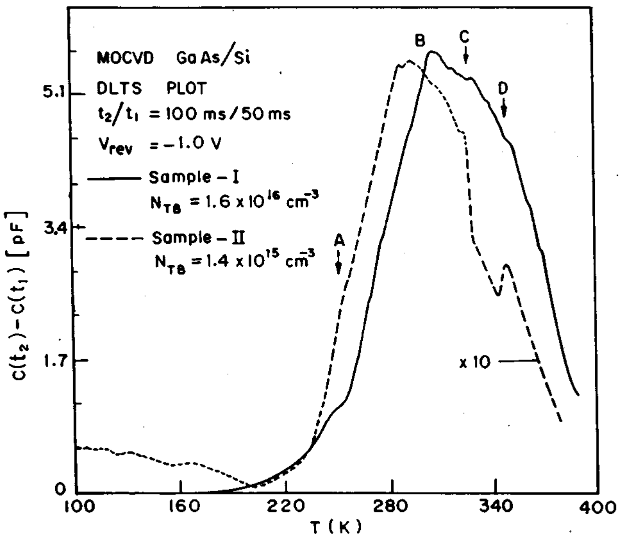


FIG. 3. DLTS spectra of electron traps in sample I and II, indicating concentration of trap B only.

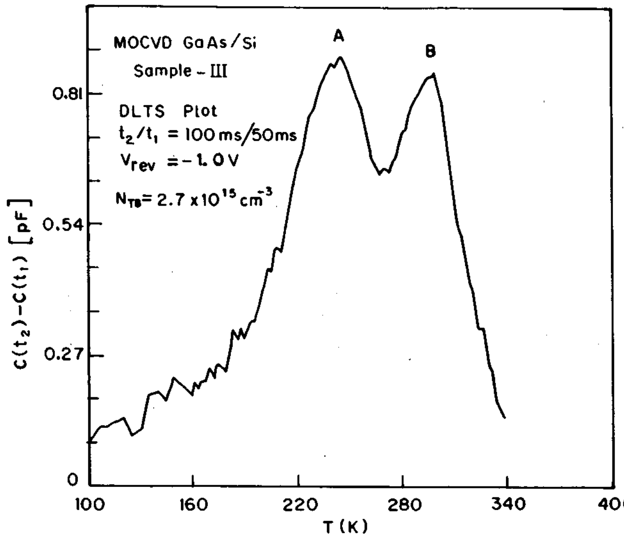


FIG. 4. DLTS spectrum of electron traps in sample III. The trap concentration shown here corresponds to that of trap B which almost equals the concentration of trap A.

SLS buffer, use of a predeposition layer grown by ALE can dramatically improve the material quality of GaAs/Si epilayers. The full width at half maximum (FWHM) of 13.8 meV of the excitonic peak in sample I is reduced to 12.4 and 12 meV, respectively, for sample II and sample III. These data are another indication that the dislocations and APDs are reduced in the latter samples.

The PL spectrum for sample II further shows the familiary ''D'' and ''E'' peaks which are related to extraneous impurity related sources.[2] The peaks are, however, not observed for sample III which, instead, contains a peak ''C,'' known to be due to the presence of residual carbon impurities.[17]

## B. DLTS

DLTS spectra for samples I and II are almost similar as is seen from Fig. 3. The main peak at ~300 K is attributed to an electron trap which we call trap B. The data also indicate the presence of three more electron traps A, C, and D, appearing as weak shoulders. Sample III, on the other hand, shows two prominent peaks, almost equal in height, due to traps A and B only and the other two traps are virtually nonexistent. These data are shown in Fig. 4 and are used to construct the Arrhenius plots for traps A and B in Fig. 5. We note that two analogous electron traps were obtained previously by Soga *et al.*[18] from DLTS studies on GaAs/Si grown by MOCVD with SLS buffers. The 0.44 eV electron trap observed by these authors, has properties similar to trap A in this study and they attributed its origin to Si defect complexes arising out of autodoped Si. However, the 0.74 eV electron trap, which they related to EL2, may be different from the trap B in our materials. Comparison of the properties of this trap with the published data of electron traps in GaAs[19] indicates that trap B may be the same as EL12, previously detected in vapor phase epitaxial GaAs. On the other hand, either of the electron traps C and D may be linked to EL2 or both may be members of the EL2 family.[20] We can also note that any EL2 like defect is either absent or is present in very low concentrations in sample III.

The concentrations of trap B in all samples and that of trap A in sample III were measured from the corresponding DLTS peak heights and they are depicted in Figs. 3 and 4. We observe that the concentration of trap B in samples II and III are, respectively, about ten and six times lower than that in sample I. We can recall that the PL intensity from these two samples increased by almost the same factors. Hence, trap B may be regarded as the main nonradiative center in these materials. From the position of the shoulder due to trap A in sample I, we can note that this trap has almost equal concentrations in both sample I and sample III. For sample II, however, trap A apparently has a much lower concentration. This result is expected in view of the studies made by

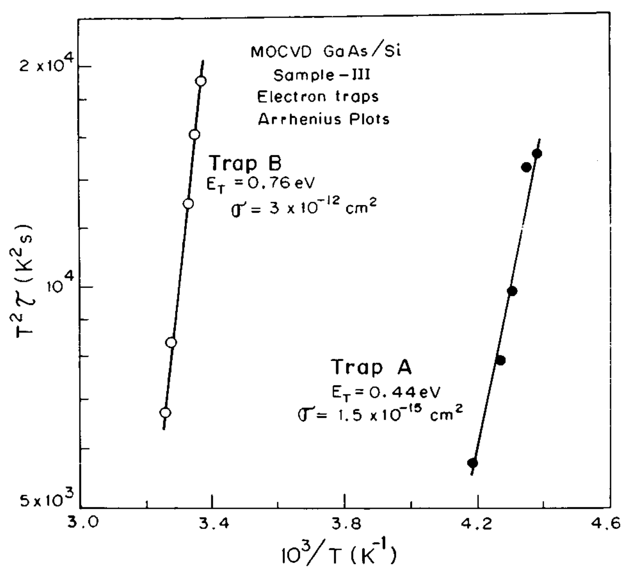


FIG. 5. Arrhenius plots for electron traps A and B, measured from the DLTS data of sample III.

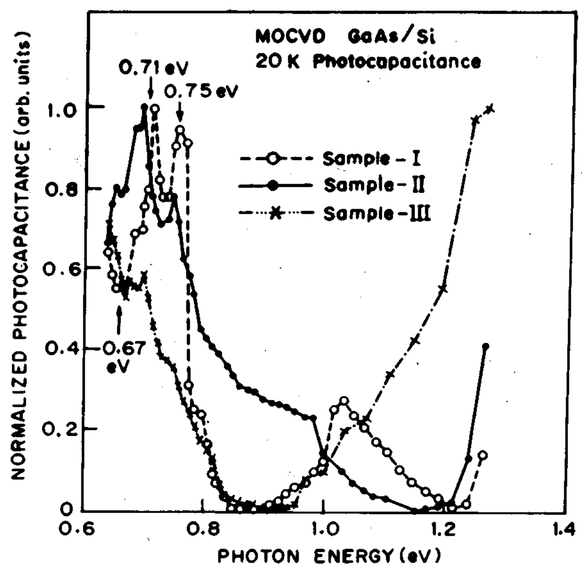


FIG. 6. Photocapacitance spectra of electron and hole traps in samples I, II, and III.

Soga *et al.*,[18] where trap A density fell with increased GaAs layer thickness. In our case, the additional SLS buffer in sample II, therefore reduces Si defect complex formation which is supposed to be the origin of trap A.

### C. Photocapacitance

Finally, we come to the analysis of our steady-state photocapacitance results which are presented in Fig. 6. These data show the presence of a number of electron and hole traps in the layer in the excitation photon energy range of 0.62–1.26 eV and are characterized by both direct and complimentary transitions from each trap level. A step capacitance rise corresponding to an electron trap level. lying 0.65—0.67 eV below the conduction band is noted in all the three samples. Magnitude of capacitance rise is, however, much smaller in sample III indicating that the electron trap is present in relatively low concentrations in this sample. Similarly we observe a sharp fall in capacitance at 1.0 eV in samples I and II only which is attributed to complementary transitions from the same electron trap. We identify this trap with the levels C[21] or ET2,[24] detected earlier in MOCVD-grown GaAs/Si. Origin of this trap is not immediately known but our results indicate that the ALE-grown predeposition layer somehow makes its occurrence less probable. The capacitance rise at 0.75 eV is linked to emission from trap B and its effect is found to be most pronounced in sample I, in agreement with the DLTS results.

From Fig. 5, we also identify two hole traps at 0.71 and 0.75 eV. While the former trap may be the same as hole trap B, detected previously in liquid phase epitaxy[22] and vapor phase epitaxy[23] grown GaAs, the latter hole trap may be identified with the hole trap HT1, found in MOCVD GaAs/Si.[24] It is apparent that these two hole traps are present in all the three kinds of GaAs/Si samples grown by us and are probably related to native defects.

## V. CONCLUSIONS

It is clear from our above studies that ALE growth of the predeposition layer gives a simple and useful alternative for getting high quality GaAs layers on Si. Layers grown by this technique show an almost sixfold increase in luminescence compared to that obtained from materials grown by a conventional two-step technique. This increase in luminescence is accompanied by a corresponding decrease in the density of an electron trap B which is supposed to be the main radiation killer. The above properties are shown to be comparable to that of layers grown with SLS buffers. We also note that, compared to the layers grown with or without SLS buffers, the ALE predeposited layer does not show the presence of any EL2 like defect.

From photocapacitance studies, we detect an additional electron trap with photoionization energy of 0.65—0.67 eV. This trap, apparently, has minimum concentration in the layers grown by our proposed technique. From the same study, we locate a 0.75 eV hole trap which seems to be a characteristic of the materials.


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