Investigation of the performance of strain-engineered silicon nanowire field effect transistors (ε-Si-NWFET) on IOS substrates

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ABSTRACT

In the current work, a design space for developing the performance enhanced strain-engineered Si nanowire field-effect-transistors has been provided. The fraction of insertion of the nanowire channel into the Insulator-on-Silicon substrate with judicious selection of high-k gate insulators is used as the key design parameter. The combined effect of fractional insertion and gate insulators results in inducing stress into the nanowire channel and, depending on their selection, it changes from tensile to compressive. Such induced-stress alters the existing inherent phononic-stress, leading to the modification of the carrier transport in the device channel. The carrier transport behavior in such partially embedded nanowire FETs has been modeled by incorporating the relevant stress-related effects into the indigenously developed self-consistent quantum-electrostatic framework. These equations are solved by employing the non-equilibrium Green's function formalism. The study shows the phonon scattering under tensile strain to occur at the expense of electron energy; however, the electrons can also gain energy during such scattering in compressive stress. Thus, the device current has been observed to increase with tensile stress and it achieves relatively smaller values when the inherent tensile phononic stress is balanced by the induced compressive stress. However, the current is finally observed to increase once the compressive stress overcomes the inherent tensile phononic stress. In general, the present devices exhibit promising I_{on}/I_{off} ratio for all of the fractional insertions and gate dielectrics with a maximum I_{off} of <10 nA/μm, threshold voltage of sub-0.3 V, g_m of ~10^4 $\mu S/\mu m$, sub-threshold swing of ~100 mV/dec, and drain-induced-barrier-lowering of ~100 mV/V.

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I. INTRODUCTION

Nanowire field-effect-transistors (NWFETs) are the potential candidates for developing future nano-electronic devices and circuits. Significant effort has been made to develop a comprehensive understanding of the transport behavior of such quantum devices,[1–6] and a few reports are also available on their successful fabrication.[7–10] However, several issues require to be addressed for the fabrication of reliable NWFETs with reproducible performance. The nanowires have extremely small dimensions with poor mechanical stability and therefore always require to be partially embedded into a substrate prior to going through the subsequent processing steps, relevant to FET fabrication. The future nanowire based circuits and systems demand the arrayed growth of semiconductor nanowires on a substrat Such nanowires will also have to be electrically isolated from each other. Therefore, such array should be grown on an insulator and the relevant insulator should be grown on the Si substrate for cost-effectiveness and process integrity. This leads to the formation of an Insulator-on-Silicon (IOS) substrate architecture. However, there will be an inherent mismatch of lattice and thermo-elastic constants between the nanowires and substrates in which these are grown/embedded. This in general leads to the incorporation of a significant amount of stress into the nanowires. Such induced stress depends on the fraction of insertion of the nanowires into the IOS substrate and also on the choice of epitaxial insulators atop the underlying Si.[11] Furthermore, the combination of materials in a FET device undergoes a

sequence of thermal cycles, and therefore, a significant amount of process-induced stress may be incorporated during such device processing.[12] The subsequent engineering of induced stress is possible by appropriately choosing constituting materials of the FET, including high-k gate-insulators and silicide contacts. The nature and amount of such stress induced during the processing along with substrate induced stress in FET devices has already been reported.[11,12–15]

Also, since the nanowires have extremely small diameters, the transport model of such nanowire FETs requires in incorporating the quantum confinement effects apparent at such scale. In this context, the comprehensive transport models in the presence of electron-phonon scattering relevant to the nanowire FET devices have also been developed.[16–18] However, the impact of induced strain/stress on the transport behavior of nanowire FETs has not yet been considered in such models. The induced stress alters band structure, carrier mobility, and phonon modes in the channel of NWFETs, depending on the value and nature of the strain, and thus, it will have an immense impact on the carrier transport. It has been reported that the Si-nanowires of the [100] orientation will not have any stress-induced effect on its carrier effective mass.[19] However, such induced stress will impart the inherent lattice vibration which will lead to the modification of electron-phonon scattering. This, in turn, changes the effective carrier mobility in the nanowire channel. Therefore, for incorporating the effect of strain in NWFETs, the existing transport model needs to be modified through the change of relevant phonon-modes. It is worthy to mention that the strain in such devices can be engineered through the judicious selection of gate materials and the fraction of nanowire insertion into the IOS substrate.[13]

In the current work, an analytical full-quantum model for the transport of strained-Si NWFETs has been developed through the incorporation of the effects of stress-induced modification and imparted into the phononic vibration modes. In this context, the quantum-electrostatic equations relevant for the current NWFETs are formulated, and the effect of strain is included by considering the deformation potential for phonon modes. Such equations are self-consistently solved by employing the non-equilibrium Green's function (NEGF) formalism, including electron-phonon scattering. The detailed studies are performed by estimating the conduction band energy, scattering-induced density of states, and the subsequent electrical performance parameter metrics of the strained-Si nanowire FETs, fractionally embedded into the IOS substrate. Emphasis has been given to investigate the impact of channel stress on Si-NWFET device performance by exploiting the controlled engineering of the fractionally inserted nanowire channel and its different high-k gate insulators.

II. THEORY

The schematic of NWFET fractionally embedded into the IOS substrate considered in the current work is shown in Fig. 1. The detailed description of such device structures along with its associated stress has already been reported.[11] The modeling of transport behavior in the NWFETs including the effects of

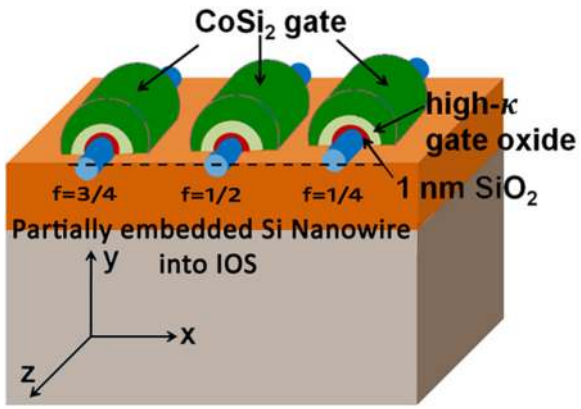

FIG. 1. Schematic of the Si NWFETs with partially embedded nanowire channels into the IOS substrate.

electron-phonon scattering[16–18] and source/drain contact resistance[5] has been elaborated by employing the relevant non-equilibrium Green's function (NEGF) formalism. However, the impact of induced stress on the performance of such devices is not yet available. In this context, the incorporation of such effects into the transport model can be performed by considering the relevant modification of Green's function due to stress related deformation. The atoms within the nanowire oscillate in discrete modes and excite/de-excite from one level to the other by absorbing/emitting a phonon, respectively. In a nanowire under strain/stress, such phonon modes get modified depending on the value as well as the nature of induced strain. This modifies the electronic transport along the device channel. The electronic transport in NWFETs is modeled by solving the quantum-electrostatic equations with a self-consistent approach and its details are available in the previous work.[16–18,20] The supply of electrons into a particular electronic state "i" is coming from the state itself, from all other possible states by absorbing/emitting phonons, and also from the source/drain reservoirs, which can be given by[18]

$$i\hbar\frac{d}{dt}c_i = H_{Iso}c_i + \sum_{j,\alpha}(\tau_{ij}^{\alpha}c_j b_\alpha + \tau_{ji}^{\alpha *}c_j b_\alpha^{+}) + \sum_r \zeta_{ir}C_r, \quad (1)$$

where H_{Iso} is the Hamiltonian of the isolated nanowire, c_i and C_r are the electron field operators at the ith and rth subband in the nanowire and the S/D reservoirs, respectively, and b_α is the field operator for phonon at α-mode with an angular frequency of ω_α. The electron-phonon interaction potential is represented by τ, and ζ indicates the coupling of the nanowire with the S/D reservoirs. Similarly, the absorption/emission of phonons in a definite mode-α is given by

$$i\hbar\frac{d}{dt}b_\alpha = \hbar\omega_\alpha b_\alpha + \sum_{i,j}(\tau_{ij}^{\alpha *}c_i c_j^{+} + \tau_{ji}^{\alpha *}c_j c_i^{+}). \quad (2)$$

The interaction potential, τ, for phonons is given by

$$\tau = D\Xi, \quad (3)$$

where D is the deformation potential of the nanowire material and Ξ is the lattice strain given by

$$\Xi = \vec{\nabla} \cdot \vec{u} + \Xi_{In}, \tag{4}$$

where Ξ_{In} is the net induced strain (both substrate and process induced). $\vec{u}$ is the lattice displacement of the oscillating atoms with wave vector $\vec{\beta}$ and can be expressed as

$$\vec{u} = \vec{u}_0 e^{i(\vec{\beta}\cdot\vec{r}-\omega t)} + \vec{u}_0{}^* e^{-i(\vec{\beta}\cdot\vec{r}-\omega t)}, \tag{5}$$

where $\vec{u}_0$ is approximated to be that for an Einstein oscillator as

$$\vec{u}_0 = \hat{v}\sqrt{\frac{\hbar\omega f_{BE}(\omega)}{2\rho\Omega\omega}}\begin{pmatrix} \frac{1}{\sqrt{2}} \\ \pm\frac{1}{\sqrt{2}} \end{pmatrix}, \tag{6}$$

where $\hat{v}$ is the polarization vector, ρ is the mass density, Ω is the normalization volume, $f_{BE}(\omega)$ is the Bose-Einstein distribution function for phonons at room temperature, and the "+" and "−" signs stand for acoustic and optical phonons, respectively. The equations can be solved to obtain the device Green's function matrix as[1]

$$[G(E)] = (E[I] - [H_{Iso}] - [\Sigma_R] - [\Sigma_{Sc}])^{-1}. \tag{7}$$

In addition, the local density of states (LDOS) for reservoirs (i.e., source and drain) and phonon scattering at each node of the nanowire channel are given by, respectively,

$$D_R(E) = \frac{i}{2\pi a} G(E)(\Sigma_R - \Sigma_R^+)G^+(E), \tag{8a}$$

$$D_{Sc}(E) = \frac{i}{2\pi a} G(E)(\Sigma_{Sc} - \Sigma_{Sc}^+)G^+(E), \tag{8b}$$

where a is the grid spacing. Finally, the 1D carrier density in the nth subband is obtained to be

$$n_{1D}^n = \int [D_S^n(E)f(E - E_{fS}) + D_D^n(E)f(E - E_{fD}) + D_{Sc}^n(E)]dE, \tag{9}$$

where $D_S^n(E)$ and $D_D^n(E)$ represent the LDOS in the nanowire channel due to source and drain contacts, respectively, and $D_{Sc}^n(E)$ is the LDOS due to electron-phonon scattering. $f(E - E_{fS})$ and $f(E - E_{fD})$ are the corresponding Fermi-Dirac distribution functions. The 1D carrier density is then incorporated into Poisson's equation for source/channel/drain potential (ϕ) after integrating it over the volume of a grid, by using the closure property of the transverse wave function, which gives rise to

$$\oint(\varepsilon\vec{\nabla}\phi)\cdot d\vec{S} = -qa\sum_n n_{1D}^n, \tag{10}$$

where ε is the permittivity of the constituent materials of the MOSFET and q is the electronic charge. For the gate architecture of cylindrical NWFETs with fractionally inserted channels, Eq. (10) leads to

$$\left[\frac{\partial^2}{\partial z^2} - \frac{2}{R^2}\frac{\varepsilon_{Ox}}{\varepsilon_{NW}}\frac{1}{\ln(1 + t_{Ox}/R)}\right](\phi - V_g) = \frac{e}{\varepsilon_{NW}(\pi - \theta)R^2}\sum_n n_{1D}^n, \tag{11}$$

where $\theta = \cos^{-1}(1 - 2f)$, f being the fraction of nanowire diameter inserted into the substrate. In the current work, the nanowire axis, i.e., the transport direction is considered to be along the z axis.

The cross section of such a fractionally inserted nanowire is schematically shown in Fig. 2. The embedded fraction of the nanowire into the substrate is assumed to be 25%, 50%, and 75% of its diameter in the present study. Therefore, the fraction, f, determines the geometric structure of the gate and effective channel cross section for the NWFETs in the current work. Equation (11) can be solved to get potential values at each node of the nanowire channel, which is then put into Eq. (1) to obtain H_{Iso}. The process is run until a self-consistency is achieved between the quantum and the electrostatic interactions. Consequently, the current components at each terminal are obtained as[18,20]

$$[I]_l = \frac{e}{h}\int\left\{\left[\sum_l^{in}(E)\right]\{i[G(E) - G^+(E)]\} - [\Gamma_l(E)][n(E)]\right\}dE, \tag{12}$$

where $[\sum_l^{in}(E)]$ and $[\Gamma_{Sc}(E)]$ denote the in-scattering function and outflow matrix, respectively. The net device current is then obtained by summing up all such current components. The components of the effective mass tensor are taken from Refs. 5 and 21 for the present calculation.

III. RESULTS AND DISCUSSION

The analytical model has been calibrated with the available experimental data for the device with similar geometry and dimensions as reported in Ref. 22. The transfer characteristics of a 10-nm channel length Ω-gate FET with a channel diameter of 10 nm and the <100> orientation are calculated and calibrated with the experimental values reported in Ref. 22. Such calibration is performed by incorporating the exact

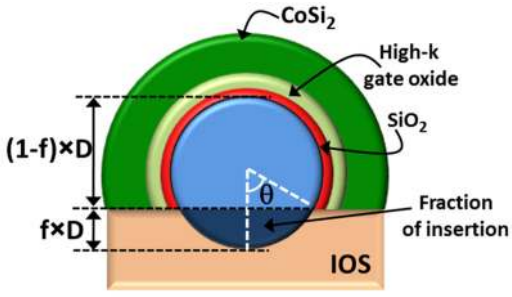

FIG. 2. Schematic representation of the fraction, f, of nanowire diameter inserted into IOS as the design parameter for the geometric structure of transistor gate and effective channel cross section.

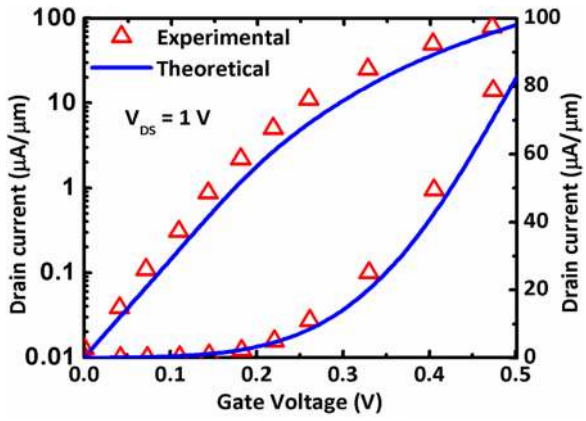

FIG. 3. Calibration of the developed theoretical model by comparing the results obtained from the theory (continuous lines) with the experimental data (scattered points) of Ref. 22.

device geometry and materials along with other relevant device parameters as reported in the experimental work. The comparative plots in Fig. 3 indicate a considerable agreement between the experimental data and theoretical values. Once the model is calibrated, then the current-voltage characteristics of Si-NWFETs with various fractions of insertion into IOS (Fig. 1) have been calculated. The channel length is taken to be 10 nm to consider the ballistic transport, and a diameter of 3 nm is taken into account for considering the quantum confinement effects, since such lateral extension is below the excitonic Bohr radius of Si.[23] The effective oxide thickness is assumed to be 2.11 nm.[11]

The stress induced into the current device structure arises from both the gate dielectrics and due to the fractional insertion of the nanowire channel into the IOS. The net amount of such induced stress for the current nanowire device dimension is calculated by following the previously reported approach.[11] In the current work, La_2O_3, Si_3N_4, HfO_2, and TiO_2 have been considered as gate insulators over the nanowire channel which is embedded into the Al_2O_3 IOS substrate. The estimated induced stress values are summarized in Table I, which are subsequently used for calculating the device parameters. Such stress values in Table I indicate its variation from tensile to compressive, depending upon the simultaneous selection of substrate, process parameters, use of gate dielectrics, and fraction of insertion.

TABLE I. Summary of the net stress ("+" stands for tensile and "−" for compressive) induced into the Si nanowire channel.

	Net stress in the Si nanowires (GPa)		
	f = 1/4	f = 1/2	f = 3/4
La_2O_3	+2.648	+0.402	−0.468
Si_3N_4	+1.948	−0.082	−0.741
HfO_2	+0.964	−0.716	−1.175
TiO_2	+0.197	−1.560	−1.911

Figure 4(a) shows the plots of variation of conduction band potential along the channel for different gate dielectrics and fraction of insertions without the application of any bias. The variation of conduction band with induced stress is observed to be almost negligible since the [100] Si nanowires have almost no impact of stress on its band curvature.[19]

Figure 4(b) shows the variation of local density of states (LDOS) (dotted lines) relevant to the electron-phonon scattering at the middle of the nanowire channel with its fraction of insertion into the IOS. It also shows the dependence of such LDOS for the use of different high-k gate dielectrics. The induced stress modifies lattice vibration and hence the phonon modes which control the net scattering probability. The "bar plots" represent the concentration of phonon-scattered electrons.

At this point, it is to be mentioned that an atom excites from its ground state to a higher state by absorbing a phonon through a corresponding dissipation of electron energy. Consequently, as the average inter-atomic distance becomes larger in such an excited state in comparison to the ground state, phonon interaction potential inherently plays the role of an equivalent tensile strain. However, when it de-excites to the ground state with the compressed inter-atomic distance, the electrons may gain energy from emitted phonons.[18] Therefore, under tensile stress, the electrons lose energy during phonon-scattering and hence higher scattering leads to current reduction. Similarly, in compressive stress, the phonons may supply energy to the electrons which leads to a current enhancement.

The variation of output characteristics of the partially embedded nanowire FETs with different high-k gate dielectrics is plotted in Figs. 5(a)–5(c), for the nanowire channels with 25%, 50%, and 75% insertion into the IOS substrate, respectively. Such current values are normalized to the corresponding effective gate perimeters. For the 25% inserted nanowire channel, the induced stress is tensile in nature ranging from 0.20 GPa to 2.65 GPa, and the increase of drain current is observed to be trivial.

However, such induced stress has a significant impact on the drain current of 50% and 75% inserted device channels. For the 75% inserted channel, the induced stress is compressive in nature which increases from 0.468 GPa for La_2O_3 to a stress value of 1.911 GPa for TiO_2 (Table I). Interestingly, the drive current, within the voltage range considered, is observed to decrease up to a stress value of 1.175 GPa and then, it increases with increasing stress. It should be noted that the drive current systematically increases, although marginally, with tensile strain; however, such systematic variation is not observed for the compressive strain. This is attributed to the inherently existing phononic tensile stress which is initially getting balanced by the induced compressive stress. During such a range of induced stress, the drive current decreases. However, when the induced compressive stress overcomes the inherent phononic tensile stress, then it

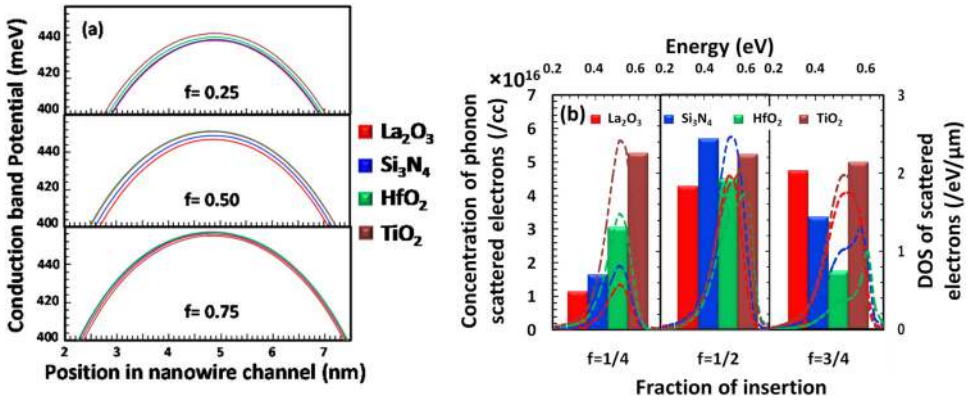

FIG. 4. Plots of (a) conduction band potential along the nanowire channel and (b) concentration (bars) and DOS as a function of energy (dotted lines) of the phonon-scattered electrons with the fraction of insertion of nanowire channels for different high-k materials.

effectively enhances the current. Such observation exactly corroborates with the results obtained in Fig. 4(b).

In contrast, for the 50% inserted channel, the induced stress is observed to change from tensile to compressive for the use of different gate dielectrics. However, the variation of drive current is observed to be similar to that of the 75% inserted channel. For La_2O_3, the stress is tensile and the drive current is the maximum. However, for Si_3N_4, the induced

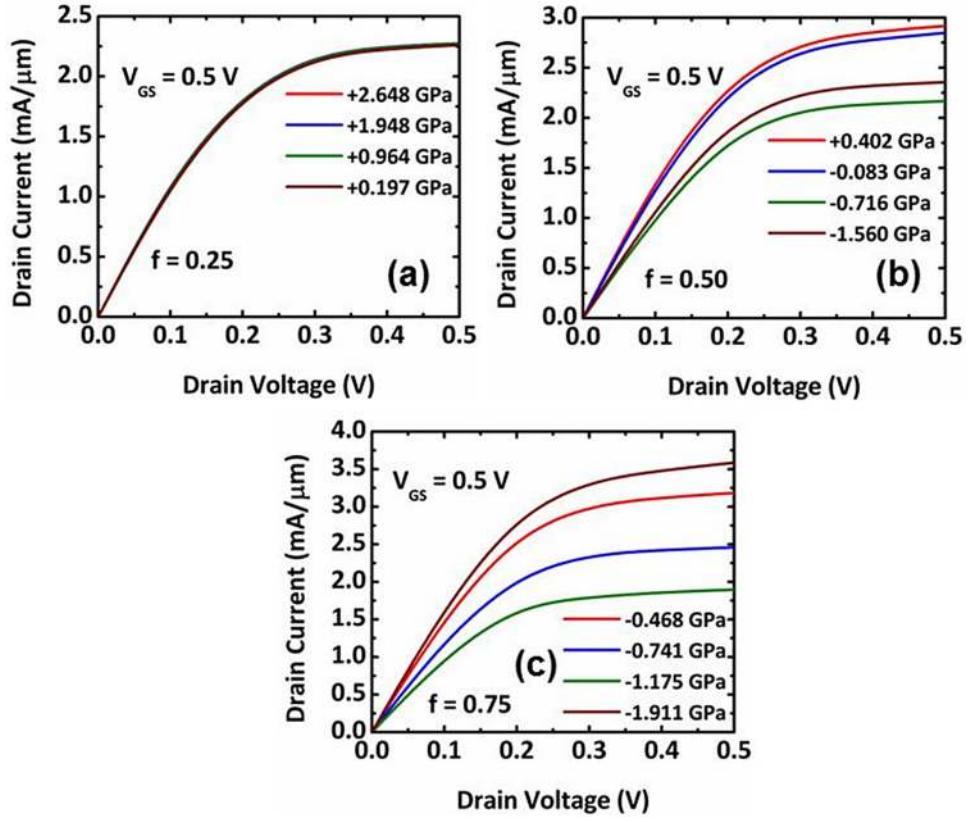

FIG. 5. The plots of output characteristics of the nanowire FETs for (a) 1/4th insertion, (b) 1/2 insertion, and (c) 3/4th insertion.

compressive stress is nominal, and thereby, the current is slightly less. When the induced compressive stress is of a similar order of the phononic tensile stress, then the net effective stress is almost zero, which results in the minimum drive current.

The transfer-characteristics (in both the logarithmic and linear scales) of the strained-Si nanowire FETs are plotted in Figs. 6(a)–6(c) for the nanowire channels with fractional insertions of 25%, 50%, and 75%, respectively.

The corresponding performance parameters for the strained-Si nanowire FETs including the on-current-to-off-current ratio (I_{on}/I_{off}), threshold voltage (V_{Th}), trans-conductance (g_m), sub-threshold swing (SS), and drain-induced-barrier-lowering (DIBL) are plotted in Figs. 7(a)–7(e), respectively, representing their variation with the induced stress for different fractional insertions.

For an increase of tensile stress from 0.20 GPa to 2.65 GPa in the 25% inserted channel, the on-current is observed to increase marginally from 2.26 mA/μm to 2.27 mA/μm; however, the off-current is increased from 5.80 μA/μm to 8.75 μA/μm, respectively [Fig. 6(a)]. Therefore, the on-current enhancement is <1%, whereas the off-current enhancement is >50% in the range of induced stress considered. However, for the 50% fractionally inserted channel, the nature as well as the value of induced stress has been observed to change from tensile to compressive in the range of +0.40 GPa to −1.56 GPa (Table I). The relevant on-current and off-current enhancements compared to their minimum values are found to be 8.75% and 14.5%, respectively. Also, for the 75% inserted channel, the induced stress is compressive in nature with the respective enhancements of ∼90% and 140%. Therefore, it is apparent from such observations that the 50% and 75% inserted channel devices will exhibit superior performance in terms of on-current to off-current ratio (I_{on}/I_{off}), which has been depicted in Fig. 7(a).

The maximum I_{on}/I_{off} is obtained for the 50% and 75% inserted channels with a compressive stress in the range of 0.716 GPa to 1.175 GPa. The threshold voltage [Fig. 7(b)] in such partially embedded Si-NWFETs is observed to vary in the range of 177 mV to 200 mV for tensile stress and under compression, it varies from 200 mV to 250 mV. The normalized trans-conductance for the 25% fractionally inserted channel marginally changes from 7.3×10^3 μS/μm to 7.9×10^3 μS/μm; however, it varies considerably from 8.2×10^3 μS/μm to 1.3×10^4 μS/μm for the 50% and 75% insertion [Fig. 7(c)]. The maximum g_m among all of the embedded fraction and gate insulator combinations is obtained for the highest compressive stress of 1.9 GPa.

The value of SS is observed to vary from 100 mV/dec to 125 mV/dec for the considered gate and substrate materials. The relatively higher value of SS is attributed to the consideration of inherent electron-phonon scattering in such

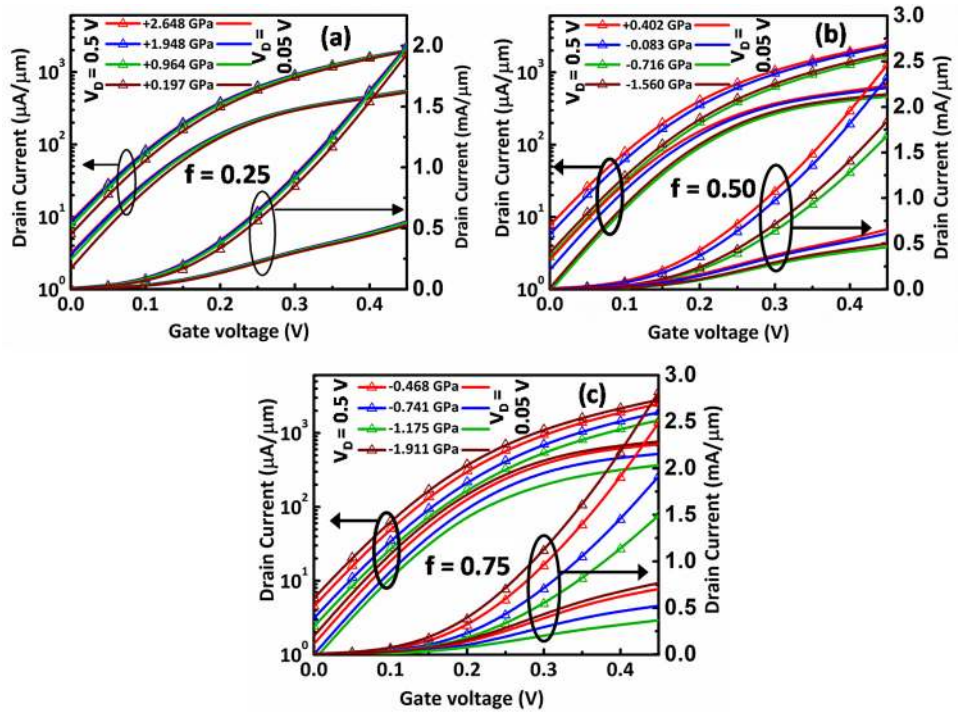

FIG. 6. The plots of transfer characteristics of the nanowire FETs for (a) 1/4th insertion, (b) 1/2 insertion, and (c) 3/4th insertion.

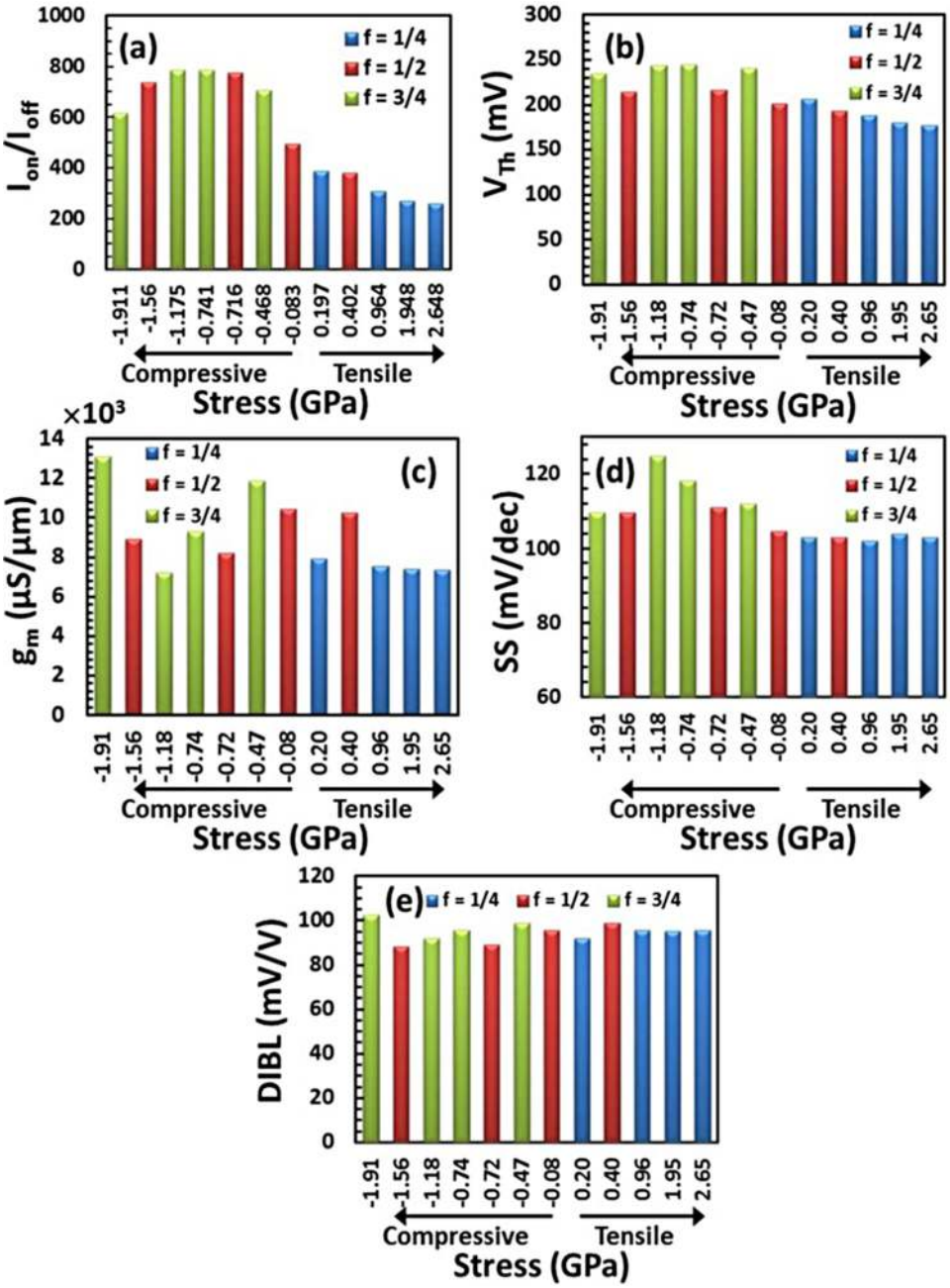

FIG. 7. The variation of (a) I_{on}/I_{off}, (b) threshold voltage (V_{Th}), (c) trans-conductance (g_m) normalized to gate perimeter, (d) sub-threshold swing (SS), and (e) DIBL of the Si-NWFETs with induced stress for various fractional insertions of the nanowire channel into IOS.

devices. In this context, it should be mentioned that the ideal value of SS (60 mV/dec) can be attained when such scattering events are neglected.[24] However, in the presence of scattering, the SS value has been obtained to be 150 mV/dec when the strain effects are not incorporated [i.e., $\Xi_{In} = 0$ in Eq. (4)], and thus, the study suggests that the induced stress improves the speed of such embedded channel NWFETs. The plots of DIBL values show a nominal variation for the combination of fractional insertions and gate dielectrics considered in the current work. The overall electrical performance parameters

TABLE II. Comparison of electrical performance parameters of Si NWFETs with partially embedded nanowire channels into the IOS substrate.

		Electrical performance parameters				
Fraction of insertion	Gate dielectrics	V_{Th} (mv)	SS (mV/dec)	DIBL (mV/V)	g_m ($\mu S/\mu m$) $\times 10^3$	I_{on}/I_{off}
f = 0.25	La_2O_3	177	103	95	7.3	260
	Si_3N_4	180	104	95	7.4	271
	HfO_2	188	102	95	7.5	306
	TiO_2	206	103	92	7.9	389
f = 0.50	La_2O_3	193	103	99	10.2	380
	Si_3N_4	201	105	95	10.4	494
	HfO_2	216	111	89	8.2	775
	TiO_2	213	110	88	9.0	736
f = 0.75	La_2O_3	240	112	99	12	706
	Si_3N_4	244	118	95	9.3	787
	HfO_2	243	125	92	7.2	788
	TiO_2	235	110	102	13.1	615

for the partially embedded channel Si-NWFETs are summarized in Table II.

IV. CONCLUSIONS

The current work investigates the performance of strain engineered Si-NWFETs for the nanowire channels with various fractional insertions into the IOS substrates and different high-k gate insulators including La_2O_3, Si_3N_4, HfO_2, and TiO_2. The electrical performance parameters such as drive current (I_{on}), off-current (I_{off}), I_{on}/I_{off}, threshold voltage (V_{Th}), SS, g_m, and DIBL have been extensively studied as the function of amount and nature of the induced stress. The analytical model for estimating the device current and its associated device physics has been developed by solving the quantum-electrostatic equations self-consistently through the formalism of non-equilibrium Green's function (NEGF). The impact of stress, induced due to partial embedding of the nanowires into IOS and the use of high-k gate dielectrics, has been incorporated in such a model. The current model modifies the phononic strain, inherently present in the lattice of Si by the substrate and process induced stress.

The conduction band energy and scattering-induced density of states are studied in detail in correlation with the incorporated stress. The energy of electrons is dissipated due to phonon scattering under tensile stress and it increases with compressive stress. The device current increases with tensile stress due to the reduced scattering-LDOS, and it also increases under net compression, however, due to energy gain by the electrons from phonons. In general, the current devices exhibit a promising I_{on}/I_{off} ratio for all of the fractional insertions and gate dielectrics with a maximum I_{off} of <10 nA/μm, threshold voltage of sub-0.3 V, g_m of ~10^4 $\mu S/\mu m$, SS of ~100 mV/dec, and DIBL of ~100 mV/V. Therefore, the current work provides a design guideline for performance enhanced strain-engineered Si-NWFETs by controlling its fractional insertion into the IOS substrate and appropriate use of gate insulators.

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