Received: 11 February 2020 | Revised: 6 June 2020 | Accepted: 23 November 2020

DOI: 10.1049/cds2.12028

IET Circuits, Devices & Systems

ORIGINAL RESEARCH PAPER

A study on flare minimisation in EUV lithography by post-layout re-allocation of wire segments

Sudipta Paul[1,2] | **Pritha Banerjee**[2] | **Susmita Sur-Kolay**[1]

[1]Advanced Computing and Microelectronics Unit, Indian Statistical Institute, Kolkata, India

[2]Department of Computer Science and Engineering, University of Calcutta, Kolkata, India

Correspondence

Sudipta Paul, Advanced Computing and Microelectronics Unit, Indian Statistical Institute, Kolkata, India.

Email: sudiptapaul2@gmail.com

Funding information

Indian Statistical Institute, under the aids of the Ministry of Statistics and Programme Implementation Govt. of India.

Abstract

The feature size in Integrated Circuits (ICs) has been scaling down aggressively, thereby posing more challenges in their manufacturability. Conventional immersion lithography using a laser of 193 nm wavelength produces layouts having distortions that degrade performance significantly. To overcome this bottleneck, Next-Generation Lithography (NGL) technologies are being developed. Extreme Ultraviolet Lithography (EUVL), one of the popular NGLs, which uses a light of 13.5 nm wavelength. However, irregularities on the photo reflective surface of clear-field masks used in EUVL, scatter the incident light and cause *flare* that in turn results in layout pattern distortions and critical dimension (CD) violations. One of the approaches to counter the effect of flare is to utilise dummy metal fills. But this incurs additional mask cost. Herein, a method to reduce the flare variation as well as the average flare distribution for a layout by perturbation of wire segments, without affecting performance at the post-layout phase, is proposed. The results show reductions of 20% and 11% on an average in the flare variation and flare mean, respectively, compared to that for the original layout for two different flare models studied on three standard sets of benchmark suites. Consequently, a reduction in the dummy fill demand of a similar magnitude is thus obtained.

1 | INTRODUCTION

IC fabrication in the current technology nodes of 14 nm, is a complex elaborate process which has evolved through many decades. Conventional immersion lithography uses a laser beam of 193 nm wavelength to print the layout *features*. However, printing sub-20 nm features without distortion is a major challenge due to the huge sub-wavelength Lithography gap [1].

Various mitigation techniques have been developed in order to continue with the immersion lithography system. Multiple Patterning (MP) [2–4] and Optical Proximity Correction (OPC) [5–7] are popular techniques to mitigate the distortions due to sub-wavelength feature printing. However, all of these mitigation techniques are reaching their limitations with aggressive scaling down of the feature size leading to the development of Next-Generation Lithography (NGLs) techniques.

A popular NGL is Extreme Ultraviolet Lithography (EUVL) with EUV light of 13.5 nm wavelength for printing sub-20 nm process technology nodes [8, 9] but the light gets absorbed by most of the substrate materials. So EUVL systems require *clear-field masks* coated with reflective material for printing on the wafer. On the clear-field mask, areas designated for the layout patterns are covered by the absorbers which absorb EUV light to print the patterns [10].

Irregularities in the reflective material on a clear field mask cause light to scatter from the vacant regions as shown in Figure 1, and is termed as *flare* in EUVL [10]. Flare changes the contrast between the dark and the bright regions, resulting in severe pattern distortions on the printed layout. Minimisation of the flare is a challenging problem for fabrication using EUVL.

The distribution of flare significantly depends on the density distribution of the layout metal patterns [11]. While uniform distribution of pattern density does not result in reduced flare over the entire layout, it is observed that flare in the central region of the chip is typically much higher than that of the peripheral regions [11, 12]. This phenomenon is referred as *flare periphery effect* [12]. Conforming the *pattern* density

This is an open access article under the terms of the Creative Commons Attribution License, which permits use, distribution and reproduction in any medium, provided the original work is properly cited.

© 2021 The Authors. *IET Circuits, Devices & Systems* published by John Wiley & Sons Ltd on behalf of The Institution of Engineering and Technology.

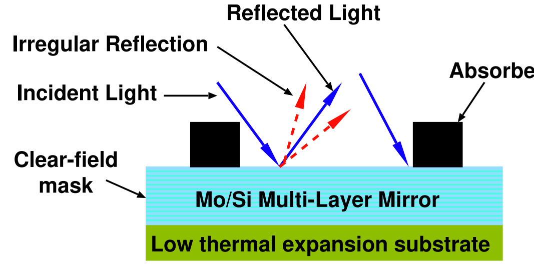


FIGURE 1 Light scattering from irregular reflective surface of the Clear-field mask

map of the layout to the *flare distribution* helps to minimise the global effect of flare. Since vacant regions are the source of flare, reduction of the vacant regions on a layout is typically used to minimise the flare. However, region filling strategies such as OPC and dummy filling incur additional mask overhead while degrading the performance of the chip. Moreover, such local mitigation techniques do not always improve the effect of flare significantly [11].

Previous works such as Refs. [10, 13] have reduced flare significantly by using extra dummy (non-functional) metal features which are typically introduced in the vacant regions to enhance mechanical robustness. However, these larger number of dummy fills increases the mask cost and the coupling capacitance between the metals if the dummies are placed without considering cross-talk as stated in Refs. [14, 15]. Effectively, this may affect the circuit speed.

In this study, the goal is to minimise flare by perturbation of already routed wire segments with no compromise in wirelength. A preliminary version of this work [16] based on Integer Linear Programing (ILP) to reduce flare by reallocation of certain post-routed wire segments, has shown promising results on a set of randomly generated small synthetic circuits but track assignment was not addressed. The main contribution reported here is the total flow for flare reduction for a given layout with the following steps:

- An ILP-based solution is obtained to reduce flare by reallocating certain routed wire segments.
- A graph-theoretic method is proposed for assigning tracks to these wire segments considering Design Rule Check(DRC).

Furthermore, the flare periphery effect has been studied with two bell-shaped pattern density distribution, namely Gaussian and sigmoidal, in the absence of an accurate model. The corresponding results of reduction in flare and estimated dummy fill requirement for the post-perturbed layouts for the circuits in MCNC, Faraday and ISPD′15 benchmark suites have been compared.

Our wire perturbation-based method can facilitate fast and cost effective migration of large volumes of highly optimised complex designs already in production under traditional Immersion Photo-lithography process at fabrcation facilities to the next-generation EUVL system. The proposed method not only preserves the original wirelength in the layout but also reduces the demand for dummy fills to reduce flare further which is corroborated by our experimental results.

The rest of the article is organised as follows. Section 2 includes preliminaries and the problem formulation. Section 3 gives the overview of our proposed method. Section 4 describes our ILP-based density redistribution method for minimisation of flare. Section 5 elaborates our post-perturbation track assignment method. Section 7 illustrates our method of relaxing the ILP to enhance the minimisation of flare. Section 6 discusses the computation of pre and post perturbation dummy demands. Experimental results are presented in Section 9 and concluding remarks in Section 10.

2 | PROBLEM FORMULATION

2.1 | Flare model

The layout to be printed is given as an image. For an EUVL system, previous researchers [17, 18] have computed flare based on the *intensity map* of layout image. The flare distribution is modelled as a *Point Spread Function* (PSF) specific to the EUVL projection system. Hence, the *flare map* of a layout is obtained from the convolution of the applicable PSF with the intensity map of the layout image. However, such computation is very time consuming. Thus the entire layout is divided uniformly into suitably sized rectangular grid cells where each grid cell is denoted as (i, j). The intensity map of the layout image is approximated to the pattern density map of the gridded layout. The values of the PSF considered are also discretised for each of the grid cells.

In the post-routing phase, the interconnection patterns of each net comprise a sequence of vertical and horizontal wire segments placed in different metal layers. Typically, each metal layer has a preferred orientation of the wire segments to be printed on it. As mentioned above, the entire area of a layout is divided into fixed sized orthogonal grid cells where each grid cell can accommodate a fixed amount of pattern area obeying the design rules, and is termed as *available area* for that grid cell. Few of the terms defined in our earlier work [16] needed to describe our proposed flow, are given below.

Definition 1 For a cell (i, j) the pattern density $D_p(i, j)$ is the ratio of the sum of areas of its existing patterns to its available area.

Definition 2 For a cell (i, j) the vacancy density is given as $D_v(i, j) = 1 - D_p(i, j)$.

For EUVL with clear field masks, as the vacant regions of the layout contribute to the flare, the vacancy density map D_v is used to approximate the intensity map, instead of the pattern density map, during computation of flare map F [10] as follows:

$$F(i,j) = D_v(i,j) \otimes PSF(i,j) \quad (1)$$

where $F(i, j)$, $D_v(i, j)$ and $PSF(i, j)$ are, respectively, the value of flare, the vacancy density and the discrete PSF corresponding to the cell (i, j) in the gridded layout.

2.2 | Problem statement

Flare mitigation can be achieved by a change in the pattern density distribution of a layout. The pattern density of the layout can be changed by either (i) introducing dummy metal fills, or ii) moving (perturbing) certain wire segments of the nets to other predefined parallel routing tracks on the same metal layer. We formulate the problem considering the latter approach of moving the segments to obtain a new pattern density map for flare minimisation without sacrificing the wirelength of the layout. Without loss of generality, ae set of patterns for wire segments on only one metal layer is processed at a time for flare reduction and referred as the layout in the remaining article. A few definitions are needed first.

Definition 3 A wire segment s in a layout is said to be movable if it can be moved to another predefined parallel routing track without increasing the wirelength of its net.

Definition 4 The perturbation range *r(s)* of a wire segment s in a layout is the set of routing tracks, parallel to s on either side of s, on which s can be moved without increasing the wirelength of its net.

A wire segment *s* which is not movable is termed as fixed. A target pattern density map D_p^t is modelled for a given layout in order to minimise flare. The goal is to achieve D_p^t by perturbation of wire segments in the layout. The problem of flare reduction by wire perturbation can be stated as in Ref. [16]:

Problem 1 *Given a uniformly gridded layout with W × H cells, the PSF and the target pattern density map D_p^t, determine the set of movable segments $S = \{s_i | 1 \leq i \leq k\}$, and re-allocate each of these to a grid cell within its perturbation range $r(s_i)$, such that the sum of the difference between the pattern density map D_p after re-allocation and the target density map D_p^t,* that is, $\sum_{i=0}^{W}\sum_{j=0}^{H} |D_p^t(i,j) - D_p(i,j)|$ *is minimised.*

3 | OVERVIEW OF OUR WIRE SEGMENT PERTURBATION

Here, an overview of the proposed method is given that includes computation of flare conforming target density map and the perturbation range of a movable wire segment. The details of ILP formulation and the track assignment are described in Section 4.

3.1 | Overview

Figure 2 illustrates the overall flow of our proposed method. A gridded layout and the relevant PSF, typically a 2D-Gaussian distribution, are the inputs. The pattern density map D_p and the corresponding vacancy density map D_v are computed from the input layout. Equation (1) is used to compute the flare map F for the input layout. In order to capture the flare periphery effect of EUVL systems, we have used bell-shaped curves, obtained from $2D$ Gaussian and sigmoidal distributions, as target pattern density maps. In the next step, all the movable segments are identified and their perturbation ranges are computed. We then employed our Integer Linear Programing (ILP) based formulation proposed in Ref. [16] with an enhancement to re-assign the movable wire segments in order to satisfy the target pattern density map with no increase in wirelength. Re-allocation of the movable wire segments to the grid cells is followed by their track assignment using an improved version of the method proposed in Ref. [19]. The new flare map is computed for the post-perturbed layout. Finally, the flare variation and the mean flare of the perturbed layout is reported. We also compute the dummy fill demand map corresponding to the pattern density map of both the input and the modified layout generated after the perturbation for comparison.

3.2 | Estimation of target pattern density

In order to guide the wire segment perturbation, a target pattern density map has to be used. Higher pattern density at the centre of the chip results in the reduction of flare due to the flare periphery effect as stated in Refs. [11, 12]. Hence, layout density needs to be high for a range over the centre and low in the peripheral region of the layout. Similar observations

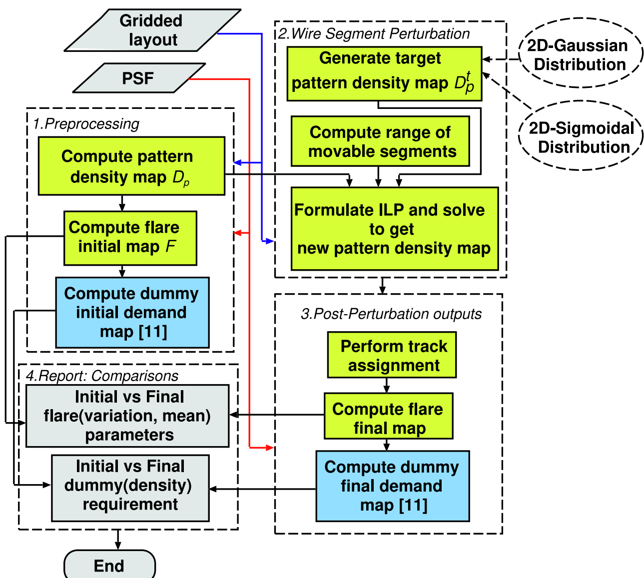


FIGURE 2 Overview of flare optimisation by wire perturbation

are also stated in previous researches such as Refs. [10, 13]. Consequently, a concave bell shaped target pattern density distribution is used to capture the flare periphery effect suitably. In this work, we have considered two models of pattern density distribution, namely, (1) Gaussian and (2) sigmoidal as considered by us in Refs. [16, 19], and studied extensively the effect on flare reduction. The Gaussian and sigmoidal distributions used for target density estimation reaches their maximum heights at the centre of the layout. The changes in the gradient of sigmoidal distribution is lower than the same in the Gaussian distribution up to a certain range from the centre of the layout. However, sigmoidal distribution changes abruptly outside that range from the centre, where as gradient of Gaussian distribution changes gradually. Figure 3(a)–(c) show the flare map of a circuit layout, a 2D-Gaussian distribution and a 2D-sigmoidal map, respectively. The similarity between the global flare distribution and the 2D Gaussian or sigmoidal distribution map justifies the use of those functions to estimate the target density map for flare minimisation.

Sections 3.2.1 and 3.2.2, respectively, illustrate the generation of target density map using Gaussian and sigmoidal function.

3.2.1 | Gaussian target pattern density

The target pattern density distribution is generated from a Gaussian function as in Equation (2), where the mean is considered to be 0. The values of i and j represent the indices of the cells in a gridded layout. Therefore, the co-ordinate system is such that the origin ($i = 0, j = 0$) lies at the centre of the chip. For a 2D normal distribution with σ as the standard deviation, it can be easily shown that the volume within 2σ distance of the mean covers 95% of the total volume of the distribution. Hence, the distance from the centre of the layout to its boundary is chosen as 2σ of the desired normal distribution for representing the flare periphery effect. This Gaussian distribution function with its maximum at the centre of the layout normalised to one is given by:

$$G(i,j) = \frac{1}{2\pi\sigma^2} e^{-\frac{i^2+j^2}{2\sigma^2}} \tag{2}$$

3.2.2 | Sigmoidal target pattern density

A sigmoidal function as given below in Equation (3) is used to generate a target density map.

$$S(i) = \frac{1}{1 + e^{-\alpha \cdot \frac{2}{\beta} \cdot (i + \frac{\beta}{2})}} \tag{3}$$

Figure 4(a)–(c) shows the steps of generating the final 2D-Sigmoidal distribution as given in Equation (4). The final sigmoidal target density map $M(i, j)$ is shown in Figure 4(c) with the maximum value at the origin, that is, at the centre of the chip.

$$M(i,j) = \frac{1}{1 + e^{-\alpha \cdot 2\beta \cdot (\sqrt{i^2+j^2} + \frac{\beta}{2})}} \tag{4}$$

In Equation (4), the parameters α and β, respectively, determine the sharpness of the curve, and the offset to translate the curve to the centre of the first quadrant. The 2D-sigmoidal curve shown in Figure 3(c) has the value of α same as that of σ in Figure 3(b).

The generation of the target density map varying the values of α and σ is revisited as explained later in Section 9 for better reduction of flare parameters.

3.3 | Computation of perturbation range

A routed net has vertical and horizontal segments laid out onto the predefined routing tracks at uniform intervals on the layout. The different segments of a net are typically connected by *vias*. A wire segment of the routed net on the layout is perturbed by shifting it to a new routing track along its original orientation without any change in its wirelength. Note that, the wirelength of a net increases if a segment having fixed pins on either side is moved in left-right (for vertical) or up-down (for horizontal) directions. Perturbation range cannot be defined for these *fixed segments*.

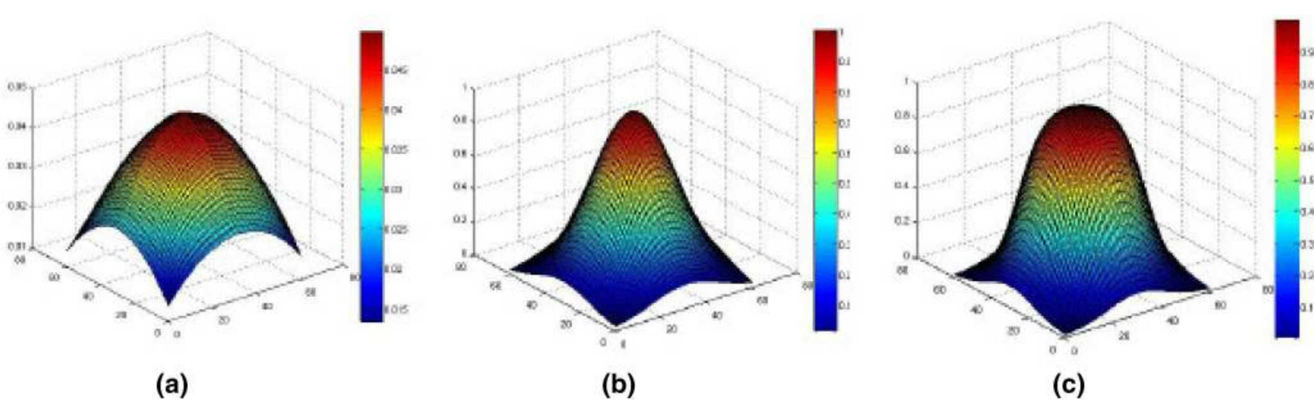


FIGURE 3 (a) The flare map of a circuit layout, (b) a 2D-Gaussian function and (c) a 2D-sigmoid function

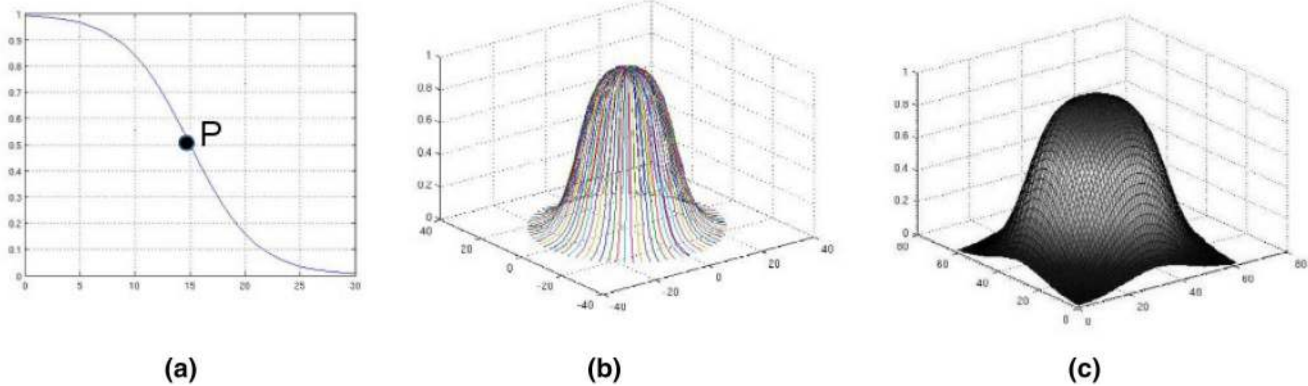


FIGURE 4 (a) A sigmoid curve with the value of 0.5 at the centre of the first quadrant; (b) Rotating the curve in (a) about the z axis; (c) Final 2D-map obtained by transforming from polar to Cartesian system

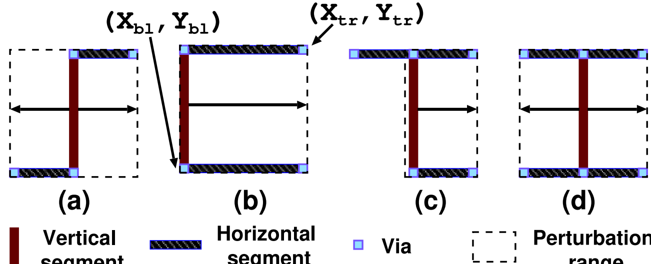


FIGURE 5 Patterns with a movable vertical wire segment; perturbation range of the vertical segment in each pattern indicated by dotted rectangle and arrows indicate permissible directions of movement

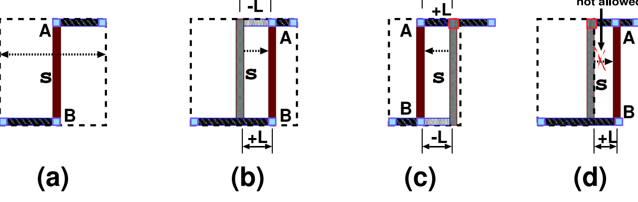


FIGURE 6 (a) Movable vertical segment s in patterns of Figure 5(a); (b) with no change in total length ($+L$ and $-L$) of net due to the left (right) movement of the vertical segment s within the dashed rectangle defining its perturbation range; (c) segment s cannot be moved to its right without increasing the wirelength due to fixed pin (marked red) but can be moved left within dashed rectangle defining its perturbation range; (d) movements not allowed due to a fixed pin

For each movable segment, we compute the perturbation range similar to Ref. [16] which preserves its wirelength. A few wirelength preserving patterns similar to Ref. [20] as shown in Figure 5 are identified for this purpose. In Figure 5, the vertical segments in all these patterns can be perturbed within a *perturbation range* X_{bl} to X_{tr}, preserving the connectivity and wirelength of the pattern.

The perturbation range is computed as the smallest rectangle enclosing a segment and the segments that are orthogonally connected to it. Once the perturbation range r_i is defined for a segment s_i, it can be moved to any valid routing track within $r_i = \{(X_{bl}, Y_{bl}), (X_{tr}, Y_{tr})\}$. Such a movement preserves the connectivity of the net and does not increase the wirelength as well. Here, (X_{bl}, Y_{bl}) and (X_{tr}, Y_{tr}) are the coordinates of the bottom left and top right corners of the perturbation range, respectively.

The effect on wirelength due to the perturbation of a movable vertical segment s within the perturbation range r is elaborated in Figure 6(a)–(d) and Figure 7(a)–(c). The figure illustrates the perturbation of vertical segments of patterns in Figure 5(a) and (b) to the left or right (dotted arrows) within the perturbation range, respectively. Note that, a wire segment is either movable or fixed depending on the presence of vias or fixed pins at its end(s).

For every pattern in Figure 5, a perturbation range can be computed similarly.

4 | PROPOSED METHOD FOR ILP-BASED WIRE SEGMENT PERTURBATION

We propose an Integer Linear Programing (ILP) based approach in order to redistribute the density of patterns on the layout conforming to the target pattern density map. As stated before, we divided the input layout into same sized rectangular grid cells for this formulation. Our ILP is formulated for each horizontal or vertical panel of grid cells. The following parameters are computed to formulate the ILP in this paper.

- The current pattern density distribution D_p computed from the input layout.
- The set of movable segments $S_P = \{s_j\}$ to be perturbed within the panel.
- The perturbation range r_j for each segment s_j as computed in Section 3.3 mapped to grid cells.
- The target pattern density map D_p^t computed using Gaussian or sigmoidal distribution as shown in Section 3.2

The objective of the ILP formulation is to minimise the flare. Hence it distributes the layout patterns such that the difference between the target density map D_p^t and the new pattern density map D_p over all the grid cells g in the panel,

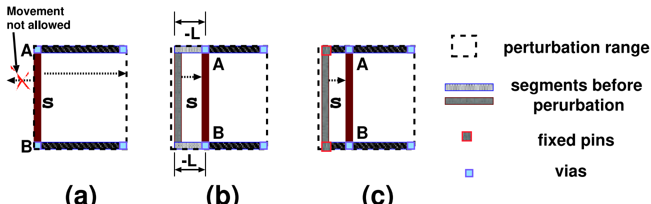


FIGURE 7 (a) Perturbation of vertical segment s in patterns of Figure 5(b) is not allowed towards left in order to preserve wirelength; (b) s can be moved right causing a 2L decrease in wirelength due to the presence of vias at both ends of s; (c) movement of s not allowed to the right due to the presence of fixed pins at both ends of s

that is, $\sum_g |D_p^t(g) - D_p(g)|$ is minimised for the corresponding panel. In order to realize the layout patterns during perturbation, all the density maps in the objective function are converted to the area maps (product of density and total area of a grid cell) in the ILP formulation.

In order to explain the ILP formulation for a panel P (vertical or horizontal) of grid cells a few notations are used as follows:

- n_c : number of grid cells in the panel
- Γ : sequence of grid cells in the panel from left to right, $<g_1, g_2, \ldots\ldots, g_{n_c}>$
- n_s : number of movable segments in the panel
- i : index of a grid cell in the panel
- j : index of a segment in the panel
- S_P : set of *movable* segments $\{s_1, s_2, \ldots\ldots, s_{n_s}\}$ in the panel P
- A_i^v : area in cell g_i available for allocation of the segments excluding the area of *fixed* segments
- A_j^s : area of *movable* segment s_j
- A_i^a : total area of the segments allocated to cell g_i given by Equation (5).
- A_i^t : target pattern area for cell g_i given by Equation (6).
- w : user defined parameter.
- x_{ij} : a binary variable defined as

$$x_{ij} = \begin{cases} 1, & \text{if segment} s_j \text{is assigned to cell } g_i \\ 0, & \text{otherwise} \end{cases}$$

For all grid cells $g_i \in \Gamma$, A_i^a and A_i^t are given as follows,

$$A_i^a = \sum_{j=1}^{n_s} x_{ij} \cdot A_j^s \tag{5}$$

$$A_i^t = A_i^v \cdot \left(D_p^t(i) \Big/ (\max_{\forall g_i \in \Gamma} D_p^t(i)) \right) \tag{6}$$

The objective function and the constraints are given in Eqs. 7 8 9 and 10 11, respectively.

$$maximize : \sum_i A_i^a - w \cdot \left(\sum_i |A_i^a - A_i^t| \right) \tag{7}$$

subject to:

$$A_i^a \leq A_i^v \quad , \quad \forall g_i \in \Gamma, \tag{8}$$

$$\sum_{i=1}^{n_c} x_{ij} = 1 \quad , \quad \forall s_j \in S_P. \tag{9}$$

$$x_{kp} + x_{lq} = 1 \tag{10}$$

The objective function in Equation (7) provides maximisation of the assigned wire segment area A_i^a in a grid cell which in turn minimises the term $A_i^a - A_i^t$. Thus, it makes the assigned segment area closer to the target area.

If the area of the segments assigned to a grid cell exceeds the available area, it causes an overflow. The constraint given in Equation (8) prevents such overflow of segment area in a grid cell.

The constraint in Equation (9) keeps the entire segment together inside a single cell. Otherwise, a segment can get split into multiple segments, requiring insertion of connecting segments in different metal layers, thus can introduce multiple design rule violations as well as additional wirelengths.

Equation (10) corresponds to the set of constraints for a pair of segments for preserving the topological order of the movable segments. The set contains constraints for each pair of segment s_p and s_q such that $s_p \in G_P$, $s_q \in G_P$ *and* $p \leq q$. Changing the order of certain pair of segments can potentially introduce overlaps (termed conflicts) during their track assignment. An example of the potential conflict that can appear in the perturbed layout after track assignment is shown in Figure 8(a) and (b) and hence taken care by Equation (10). The vertical segments s_1 and s_2 in Figure 8(a) belong to two different nets in the metal layer M_i and can move either to the left or to the right within their perturbation range. Both their connected horizontal segments h_2 and h_4 belong to the metal layer M_j. The order of the segments s_1 and s_2 is reversed due to perturbation along dotted arrows causing overlapping of h_2 and h_4 as shown in Figure 8(b).

In the set of constraints represented by Equation (10), $x_{kp}(x_{lq})$ is a binary variable which is 1 if the left(right) vertical segment $s_p(s_q)$ is assigned to grid cell $g_k(g_l)$, and 0 otherwise. Segments s_p and s_q are the vertical segments that cause conflicts if their order is changed. The indices k and l take the indices of grid cells from the perturbation range of s_p and s_q, respectively. Note that, the reversal of segments are represented only by the constraints where $k > l$.

A conflicting pair of segments in a metal layer M_i can be identified by following conditions:

- At least one of the corresponding end point is collinear;
- Perturbation ranges of both segments overlap;
- The corresponding connected orthogonal segments belong to the metal layer M_j and M_k, such that one of the following is true (i) $j, k \leq i$ or (ii) $j, k \geq i$ or (iii) $j = k$.

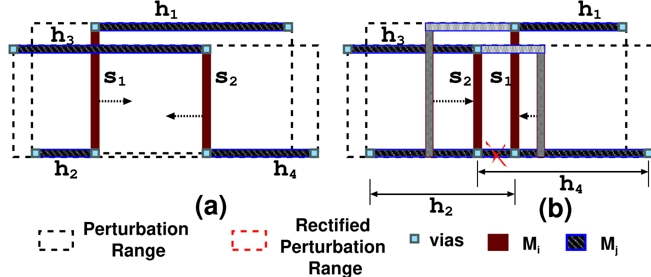


FIGURE 8 (a) Patterns with conflicting horizontal segments h_2 and h_4 of two different nets in M_1 within the perturbation range of vertical segments s_1 and s_2 in M_2. (b) Conflict between h_2 and h_4 due to reversal of the order of s_1 and s_2 within the perturbation range

Our objective function is piece-wise linear as it contains modulus. The objective function is approximated to a linear function as in Ref. [21]. Let $X' = |A_i^a - A_i^t|$ in the objective function (Equation (7)). In order to linearise the objective function, two more constraints are added as given in Eqs. 11 and 12.

$$(A_i^a - A_i^t) \leq X_i', \forall g_i \in \Gamma \tag{11}$$

$$-(A_i^a - A_i^t) \leq X_i', \forall g_i \in \Gamma \tag{12}$$

The final objective function is,

$$maximize : \sum_i A_i^a - w \cdot \sum_i X_i' \tag{13}$$

5 | TRACK ASSIGNMENT OF RE-ALLOCATED SEGMENTS

The ILP formulation for perturbation of wire segments redistributes the movable segments in order to conform to the target pattern density. Hence, the result of our ILP provides only the assignments of a set of wire segments tot he given grid cells. The perturbed wire segments need to be assigned to the available *free intervals*, denoted by (y^{tp}, y^{bt}), on tracks in the designated grid cells preserving the design rules. The free intervals are computed considering the fixed segments that are already placed entirely or partially on a track in a panel. We developed a method based on bipartite graph matching, similar to Refs. [19, 22], to assign wire segments to tracks within each grid cell. The segments that fail to obtain a free interval by bipartite matching are then assigned to tracks using a local refinement method. Note that, we have taken care of design rules for vias and metal wires spacing during perturbation and track assignment. Brief explanation of the implementation details are also added in the later part of this section.

5.1 | Track assignment by bipartite matching

A bipartite graph $B_g(U \cup V, E)$ is constructed for each grid cell g where:

- $U = \{u_i\}$, $1 \leq i \leq m$: u_i corresponds to a wire segment assigned to the grid cell g by ILP.
- $V = \{v_j\}$, $1 \leq j \leq n$: v_j corresponds to a free interval on a routing track in g.
- $E = \{e(i, j)\}$: edge (u_i, v_j) exists if the length of the interval corresponding to v_j is greater than the segment u_i and v_j is within the perturbation range of segment u_i in g.

A maximum matching on the bipartite graph $B_g(U \cup V, E)$ constructed for each grid cell g is performed in order to obtain the assignment of all movable segments to tracks.

Figures 9(a) and (b) and 10(a)–(c) illustrate an example of track assignment. Figure 9(a) presents a row with three grid cells g_1, g_2 and g_3, and the list of wire segments assigned to them. The perturbation range of their segments are shown as blue dotted rectangles. It may be noted that some of the tracks are occupied by the fixed segments. For example, t_3 is partially occupied by a fixed segment which is in the perturbation range of u_2. Consequently, t_3 cannot have a free interval for u_2 in spite of being within its perturbation range. Figure 10(a)–(c) shows the bipartite graphs for g_1, g_2 and g_3, respectively, along with the assignment of segments to free intervals by bipartite matching. Figure 9(b) represents the final layout after track assignment by bipartite matching.

5.2 | Track assignment for unmatched segments

The bipartite matching given above may not succeed in assigning all segments to tracks due to dearth of free intervals of adequate length in the assigned grid cell. In Figure 11(a), two segments u_1 and u_2 are assigned to the grid cell g_2 by the ILP, and both have edges to the same interval v_1 in the bipartite graph. As a result the maximum matching fails to find a track assignment for u_2. Although g_2 has enough total free area to accommodate u_2 in it, the entire length u_2 does not fit in a single free interval due to the presence of fixed segments in g_2.

In order to assign such unmatched segments to tracks, we use a local rectification strategy, as shown in Figure 11(b), by applying one of the following two options: (1) split the segment into two adjacent tracks with an appropriate connection obeying design rules for all the grid cells in a panel, or (2) allocate the segment into an interval available in an adjacent grid cell within the perturbation range of the segment. Option (1) is preferred over Option (2), even though the wirelength may increase by one pitch unit due to insertion of an extra metal segment. In Option (1), the grid cell assignment generated by the ILP is preserved. Option (2) is applied when option (1) fails to assign the segments into tracks.

The problem of a segment not being assigned to a track potentially may still exist even after using options (1) or (2). However, the track assignment for all of the circuits in the three standard benchmark suites has been completed successfully using bipartite matching followed by the above

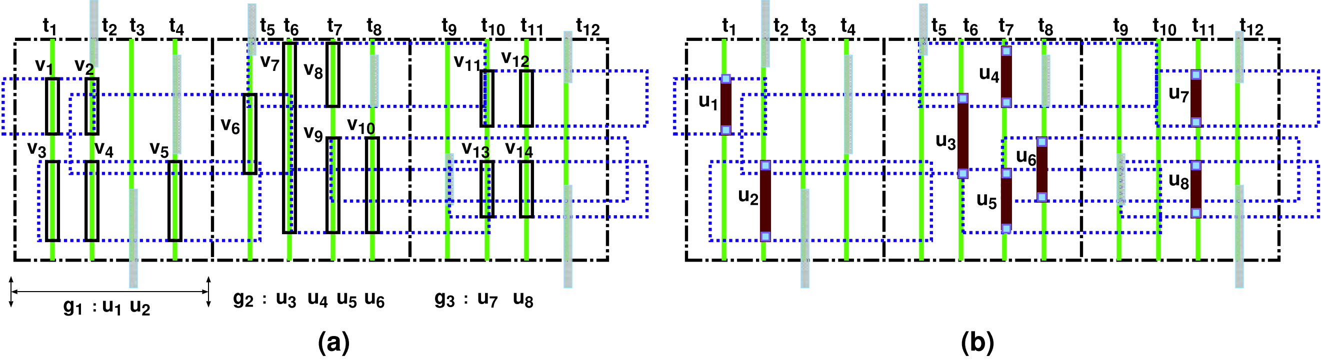


FIGURE 9 Example of track assignment: (a) Three grid cells g_1, g_2 and g_3 in a row, with segments u_1 and u_2 assigned to g_1; u_3, u_4, u_5 and u_6 to g_2; u_7 and u_8 to g_3. Intervals v_1 to v_5 in g_1, v_6 to v_{10} in g_2, and v_{11} to v_{14} in g_3 are free. (b) Final layout after track assignment by bipartite matching

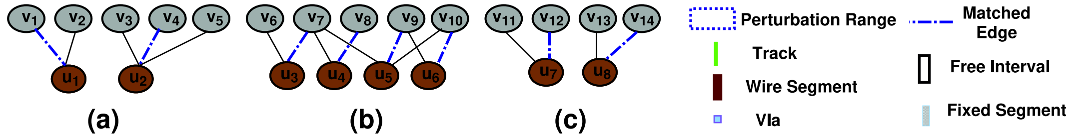


FIGURE 10 Example of track assignment: (a)-(c) Bipartite graphs for grid cells g_1, g_2 and g_3, respectively, along with the assignment of segments to free intervals by bipartite matching in order to generate the final layout in Figure 9(b)

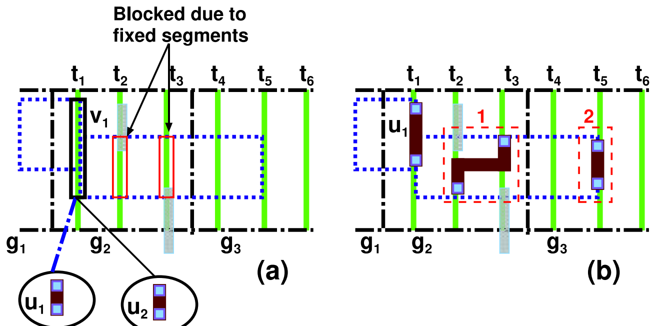


FIGURE 11 Assignment of unmatched segments to tracks: (a) in g_2 segment u_1 is matched to v_1 but u_2 is not. (b) Option (1)—split u_2 into two adjacent tracks in the same grid cell g_2 with an appropriate connection obeying design rules; if this fails, Option (2)—assign u_2 to the nearest available track in the neighbouring grid cell g_3

rectification strategies. We have reported the number of times Option (1) or Option (2) has been used later in Section 9.4.

5.3 | Avoiding DRC violation in via spacing

We have maintained the design rules during track assignment of the segments. Since routing tracks are placed with a pitch distance gap among them, wire segments placed on those tracks cannot incur design rule violations. However, we explicitly maintained the via spacing rules during assignment of the segments to the tracks using bipartite matching based method and also for the assignment of unmatched segments. Figure 12 illustrates the way we have maintained the via spacing rule in our implementation. Via B has proper spacing with via A only if it is placed on the position marked as Pos-4. The positions denoted by Pos-1, Pos-2 and Pos-3 are invalid for the placement of via B with respect to via A.

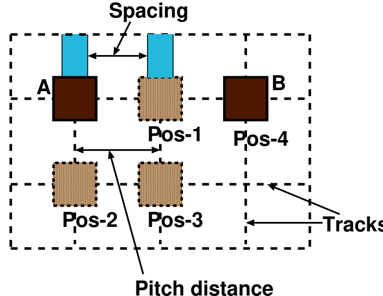


FIGURE 12 Via Spacing Rule: Pos-1, Pos-2 or Pos-3 has incorrect spacing for placement of via B which can be placed only at Pos-4

6 | COMPUTATION OF DUMMY DEMAND

The flare in EUV lithography can also be reduced by introducing extra dummy metals in the layout as proposed earlier in Refs. [10, 11, 13]. However, dummy metals can cause interference with metal wire segments for signal nets, resulting in increased coupling capacitance or crosstalk [14, 15, 23]. In Ref. [23], the authors have proposed a formulation of the coupling capacitance for various types of dummy fills. The study in Ref. [14] uses a pre-computed look-up table for coupling capacitance between two metal fills with respect to their distance.

Thus introduction of additional dummy fills compromises the effectiveness of flare reduction.

The redistribution of density on the layout by our ILP-based wire perturbation decreases the flare on the layout. For further decrease in flare, dummy metals can then be added along the lines of the earlier works. In order to study the effects of wire perturbation followed by dummification on a layout, dummy fill demand is computed as in Ref. [10]. The flare map and the PSF are the inputs. Flare on a layout surface is a global phenomenon. The flare of one grid cell is affected by that of its neighbouring grid cells. Hence, quasi-inverse lithography technique [5] is used to model the propagation of dummy demand of neighbouring cells to a grid cell. The quasi-inverse PSF is generated by the convolution of the PSF with itself as shown in Equation (14).

$$PSF_Q(i,j) = \sum_f \sum_g PSF(f,g) \cdot PSF(i-f, j-g) \quad (14)$$

Next, the dummy demand density map is obtained by convolution of the flare map and the quasi-inverse PSF map using Equation (15).

$$Dummy(i,j) = \sum_f \sum_g F(i-f, j-g) \cdot PSF_Q(f,g) \quad (15)$$

Here, f and g run over all the values that lead to legal subscripts in both Eqs. 14 and 15 for the inputs under consideration. First, the initial dummy demand density map is computed with Equation (15) for the initial layout. Next, two final dummy demand density maps are generated for each final layout obtained after wire perturbation by ILP followed by track assignment considering (a) Gaussian, and (b) sigmoidal target pattern density maps. Finally, the initial dummy demand map is compared with the two final dummy demand maps to study the reduction in dummy demand due to wire perturbation. The results of the experiments given below in Section 9 indicate that the dummy fill demand after wire perturbation significantly reduces, thereby resulting in lower dummy cost compared to that for flare reduction by dummification alone.

7 | IMPROVED FLARE REDUCTION BY ILP WITHOUT ORDER PRESERVING CONSTRAINTS

The ILP solution gives order preserving assignments of wire segments in grid cells by the constraint given in Equation (10) such that the values of flare are minimised. Since the ILP is solved at grid level with no track information, it does not assign any conflicting pair of segments to the same grid cell although it is observed that the order of those segments can be preserved in the same grid cell provided the track information is given. This over-restriction results in less reduction in flare. Furthermore, the order preserving constraints in the ILP slow down the solver. Hence, relaxed version of the ILP which is without the order preserving constraints is also solved to speed up the method and to further enhance the flare reduction. In order to improve the solution quality and resolve conflicts, the conflicting pair of segments are pre-processed to preserve the order.

Conflicting pairs of segments are identified by following the three criteria given in Section 4, and their corresponding perturbation ranges are shrunk accordingly such that these ranges do not overlap any more. This scenario is explained in Figure (13a) and (b). Then those segments are assigned to tracks as any other segment during track assignment. In Section 9 below, the results of flare reduction by using this relaxed version of ILP are referred as *Relaxed ILP*.

8 | COMPLEXITY ANALYSIS OF OUR PROPOSED METHOD

Our proposed method of wire perturbation is based on ILP which is NP-Complete. We have used *lp_solve* package which uses primal simplex method and branch and bound technique for finding the optimal solution. For our track assignment step by bipartite matching, we have used the networkX library which uses Hopcroft-Karp algorithm. Hence, the runtime complexity of our track assignment step is $O(|E| \cdot \sqrt{(|U| + |V|)})$ [24], where bipartite graph $B(U, V, E)$ is constructed for each of $W \times H$ grid cells.

9 | EXPERIMENTAL RESULTS

The proposed method is implemented using C on a system having Intel(R) Xeon(R) CPU E5-2609 v2 @ 2.50 GHz processor and 24 GB memory. The PSF used in flare computation is modelled as the 2D-Gaussian distribution function. The convolution function in MATLAB [25] is used for computation of flare and dummy maps. The user defined balancing parameter w is set to 0.5 to balance the objective function of ILP for maximisation of segment assignment, and the minimisation of the gap between the assigned and target area map. The standard library *lp_solve* package [21] is used to solve the ILP. Since the central area of the chip contributes to a higher level of flare than the periphery, the ILP for the middle panel is solved first. The method processes panels starting from the centre and then gradually the periphery in subsequent iterations. Finally, flare variation (computed as the difference

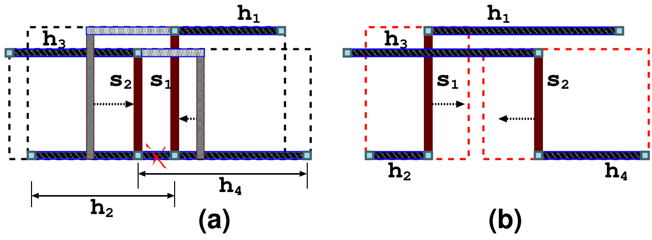


FIGURE 13 (a) Conflict resolution by restricting perturbation ranges, (b) Conflict is resolved by restricting the perturbation ranges of s_1 and s_2

between maximum and minimum flare) and mean flare are reported corresponding to both Gaussian and sigmoidal target density maps. In addition to that, we have used the Python networkX library [26] to solve the maximum bipartite matching problem for the track assignment.

We have performed our experiments on fully routed circuits of three standard benchmark suites MCNC [27, 28], FARADAY [29, 30] and ISPD 2015 [31]. Moreover, it is implicit to state that our formulation is applicable to any value of pitch distance for the circuits. Hence, the formulation will remain same for any technology nodes. Our experiments were performed only for the vertical metal layers. However, the method is applicable to the horizontal metal layers also, keeping the vertical segments fixed.

Choosing a Suitable Target Density Map: In our experiment, we have kept the PSF fixed, generated with a value of σ equal to one fourth of the size of the layout. For this example, the value of σ used in the PSF is 15 for a 61 × 61 grid layout. However, we revisit the estimation of target pattern density map presented in Section 3.2 in our experiment to enhance the reduction in flare. The value of the standard deviation (σ) is varied in order to change the 2D-Gaussian target density map. The 2D-sigmoidal target density map is similarly revisited for the same reason by modifying the sharpness of the function controlled by the value of α. It has been observed that the value of σ of Gaussian target density map closest to that of PSF, gives best results for the benchmarks considered by the proposed method. Moreover, an α with a value equal to σ of PSF provided the best result for minimisation of flare. Increase or decrease of σ and α was found to be degrading the reduction of flare as shown in Figure 14.

The experimental results presented in the paper for $L \times L$ gridded layouts uses the value of σ as $\frac{1}{4}L$ for Gaussian target density map to enclose the central region of the layout within 2σ as explained in Section 3.2.1. The value of α for the sigmoidal target density also uses the same value, whereas β is assigned to $\frac{-L}{2}\sqrt{2}$ to translate the centre of the distribution to the origin as explained in Section 3.2.2.

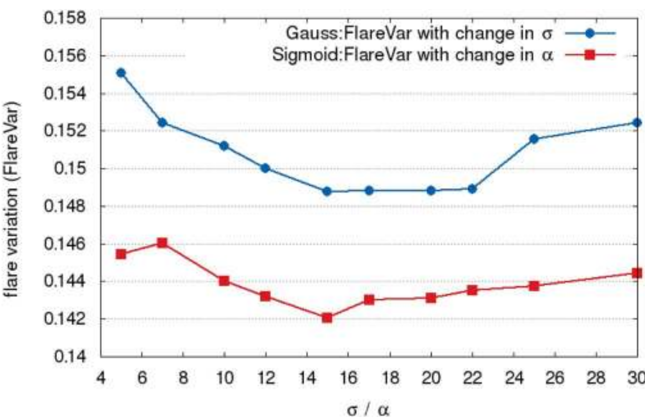


FIGURE 14 Reduction of flare variation (Y-axis) versus standard deviation σ and parameter α (X-axis) of Gaussian and Sigmoidal target density map, respectively, for a 61 × 61 grid layout of the circuit *DSP*2 in Faraday benchmark suite

Section 9.1 presents the detailed specifications of the benchmark suites. Section 9.2 elaborates the experimental results using the Gaussian and sigmoidal target density map, respectively. The dummy demands at the post-perturbation stage is reported and compared with the dummy demands of the initial layout in Section 9.3. Finally, Section 9.4 gives a summary of our results.

9.1 | Description of the benchmark circuits

Tables 1 to 3 specify the details of MCNC, FARADAY, and ISPD′15 benchmark circuits, respectively.

In Tables 1 to 3, the columns headed *Circuit*, *Area*, *#Nets*, show the name of the circuit, die area in μm^2 and the total number of nets in the circuit, respectively. The MCNC circuits in Table 1 have three metal layers in each case, *M*2 being the vertical layer. The Faraday circuits in Table 2 have six metal layers with *M*2, *M*4 and *M*6 being the vertical layers. Each of the ISPD′15 circuits in Table 3 has five metal layers, *M*2 and *M*4 being the vertical layers. The columns *Nets_M*2 and *Segs_M*2 in Table 1 represents the number of nets with wire segments in the corresponding metal layer and total number of segments in that metal layer. The remaining Tables 2 and 3 report the same as a pair (*#Nets*, *#Segs*) in the column under corresponding metal layers.

9.2 | Results for wire perturbation-based flare minimisation

A detailed study on flare minimisation is reported by applying our proposed method for wire perturbation and track reallocation on the three sets of benchmark suites with Gaussian and sigmoidal target density maps generated as illustrated in Sections 3.2.1 and 3.2.2, respectively. Table 4 shows the initial and final pattern density and flare maps obtained by our proposed wire perturbation method for the three circuits *DSP*2, *s*13207 and *mgc_edit_dist* selected as

TABLE 1 Specifications of MCNC benchmark circuits

Circuits	Area(μm^2)	#Nets	#Nets_M2	#Segs_M2
s13207	660 × 365	3778	3765	8518
s15850	705 × 389	4471	4446	10,022
s38584	1295 × 672	14,754	14,721	33,306
s38417	1144 × 619	11,309	11,281	24,808
s5378	435 × 239	1694	1689	3788
s9234	404 × 225	1478	1476	3284
Struct	4903 × 4904	1920	1593	5361
primary1	7522 × 4988	904	852	3521
primary2	1040 × 6600	3029	2727	14,710

TABLE 2 Specifications of FARADAY benchmark circuits

Circuit	Area (μm^2)	#Nets	M2 #Nets,#Segs	M4 #Nets,#Segs	M6 #Nets,#Segs
DMA	408 × 408	13,256	9756, 42489	3233, 8229	619, 958
DSP1	706 × 706	28,447	22622, 85282	6449, 15778	1157, 1934
DSP2	643 × 643	28,431	22502, 84253	6518, 16042	837, 1297
RISC1	1004 × 1004	34,034	27914, 133475	8549, 26597	1572, 3028
RISC2	960 × 960	34,034	27696, 132340	8450, 28856	1781, 3388

TABLE 3 Specifications of ISPD′15 benchmark circuits

Circuit	Area (μm^2)	#Nets	M2 #Nets,#Segs	M4 #Nets,#Segs
mgc_des_perf_1	445 × 445	112,878	94716,400984	26174,86235
mgc_des_perf_a	900 × 900	110,281	85054,355020	20259,78369
mgc_des_perf_b	600 × 600	112,878	85106,304736	20528,60074
mgc_edit_dist_a	800 × 800	131,134	112503,1040607	37600,327549
mgc_fft_1	265 × 265	33,307	28044,127886	6718,28072
mgc_fft_2	342 × 342	33,307	27538,160284	4752,25708
mgc_fft_a	800 × 800	32,088	26828,122397	5201,26284
mgc_fft_b	800 × 800	32,088	25555,134879	5682,34861
mgc_pci_bridge32_a	400 × 400	29,985	18098,85672	3704,21798
mgc_pci_bridge32_b	800 × 800	29,417	20123,74729	3773,13444

TABLE 4 Example of initial and Final pattern density map and flare map

	Pattern Density Map		Flare Map		
Initial	Gaussian	Sigmoidal	Initial	Gaussian	Sigmoidal
MCNC Benchmark Circuit: s13207					
FARADAY Benchmark Circuit: DSP2					
ISPD′15 Benchmark Circuit: mgc_edit_dist_a					

examples from FARADAY, MCNC and ISPD′15 benchmark suites, respectively. These results are for vertical metal layer M_2 only.

Wire perturbation using sigmoidal target map shows more significant minimisation in flare levels than that with Gaussian target density map. Appendix I (Table A1) presents the results

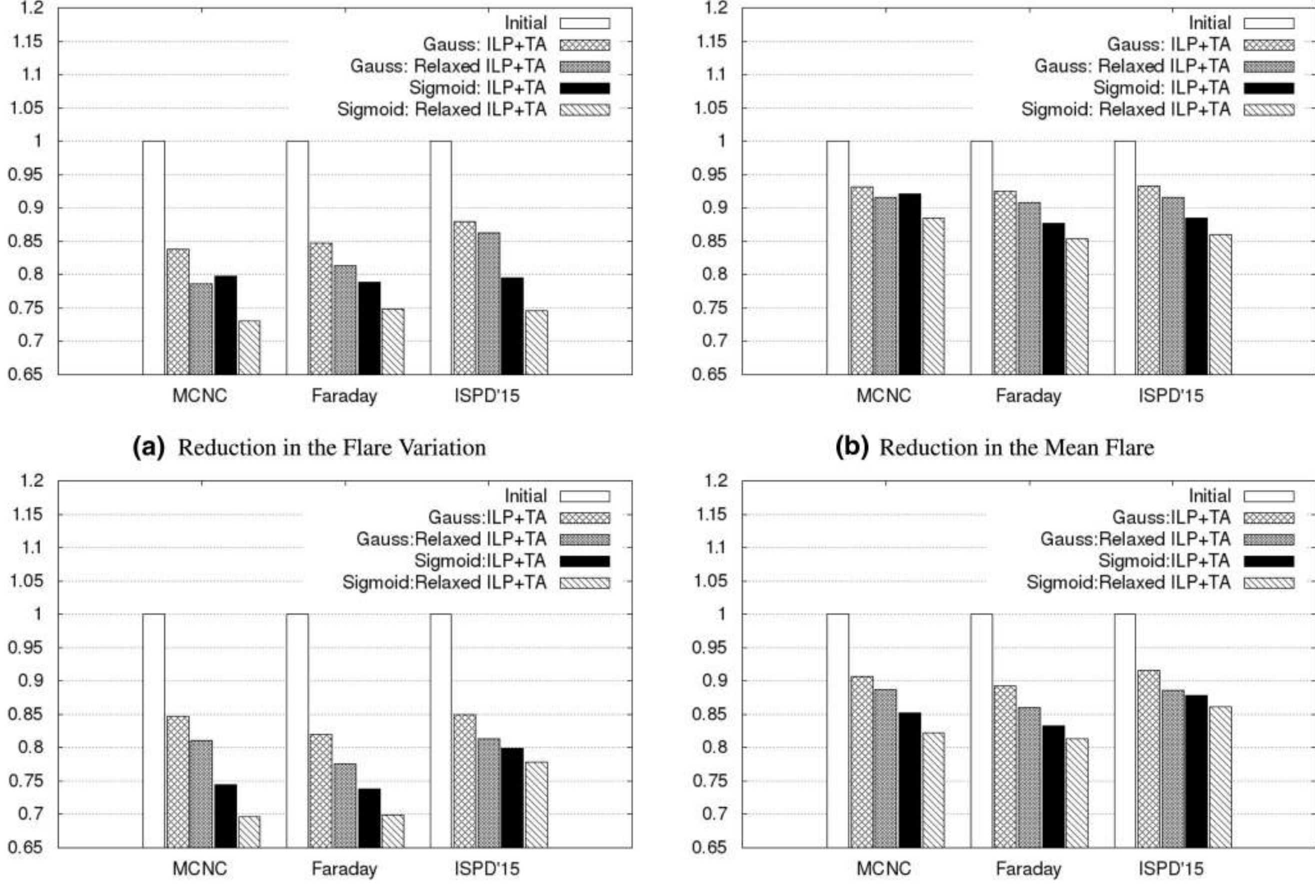
in detail for minimisation of flare with Gaussian and sigmoidal target density map. A summary is given in Figure 15(a) and (b) as plots of the normalised reduction using Gaussian and sigmoidal target density map of flare variation and flare mean for metal layer $M2$ of each of MCNC, FARADAY and ISPD′15 benchmark suites, respectively.

It can be seen that on average 14% and 18% reduction in flare variation compared to the initial layout for metal layer $M2$ over all three benchmark suites is obtained as a result of our ILP-based and relaxed ILP-based methods, respectively, using Gaussian target density map. In case of sigmoidal target density map, on average 21% and 26% reduction in flare variation is achieved for the same methods, respectively. Similarly, on average 7% and 8% reduction in flare mean for metal layer $M2$ is obtained for ILP-based and relaxed ILP-based methods, respectively, using Gaussian target density map. However, when using the sigmoidal target density map, about 10% and 12% reduction on average can be achieved in flare mean similarly. It can also be observed from Table A1 that the reduction of flare variation and mean is highest in the vertical metal layer $M2$ and gradually decreases for the upper metal layers.

9.3 | Results for post-perturbation dummy demand

Next, we have studied the reduction in dummy fills demand on the post-perturbed layout compared to the initial layout, as described in Section 6. Appendix II (Table A2) has the results for the circuits in all three benchmark suites. A summary is given in Figure 15(c) and (d) as plots for the normalised reduction over all circuits in each benchmark using Gaussian and sigmoidal target density maps.

Results of our ILP-based and relaxed ILP-based methods, using Gaussian target density map show, on an average a reduction of 16% and 20% in dummy demand variation compared to the initial layout for metal layer $M2$ for all three benchmark suites. Similarly, on an average a reduction of 24% and 27% in the dummy demand variation is achieved using sigmoidal target density map for the same methods, respectively. The dummy demand mean reduces 9% and 12% on an average for ILP-based and relaxed ILP-based methods, respectively, using Gaussian target density map, whereas sigmoidal target density map obtains a reduction of 15% and



(a) Reduction in the Flare Variation

(b) Reduction in the Mean Flare

(c) Post-Perturbation Reduction in the Dummy Demand Variation

(d) Post-Perturbation Reduction in the Mean Dummy Demand

FIGURE 15 (a, b) Summarised results of flare reduction by ILP-based wire perturbation followed by Track Assignment (TA) of re-allocated segments for circuits of three different benchmark suites: x-axis represents the three benchmark suites MCNC, Faraday and ISPD′15; y-axis represents the reduction for (a) Flare variation and (b) Mean flare compared to the initial layout. Each value is normalised with respect to the initial values. (c,d) Similarly summarised result for reduction in dummy demand variation and mean dummy demand for all three benchmark suites

17% in the mean dummy demand on average reduction for the same methods.

9.4 | Summary

The results of our study established significant decrease in flare values by the proposed method of perturbing the wire segments.

Our observations from this study are listed as follows:

- The global flare distribution depends on the density distribution of the layout patterns. Minimisation of flare by density redistribution method depends greatly on the target pattern density map. Our study with two different types of bell-shaped target density map explores the strength of choosing an appropriate target pattern density model for flare minimisation. As described in the Section 3.2, the sigmoidal distribution has slower change in the gradient within a certain range around the centre, compared to the Gaussian distribution. Hence, the volume under the sigmoidal distribution is more compared to Gaussian distribution within that range. As a result sigmoidal distribution accommodates more layout patterns within the said range around the centre of the layout. The results clearly show that a sigmoidal target pattern density map reduces flare more than a Gaussian map.
- The segment ordering of conflicting pairs are preserved either by certain constraints in the ILP or by modification in the perturbation ranges. Removal of the order preserving constraints along with restriction of perturbation ranges led to better reduction in flare and on an average 40% reduction in the time requirement, as observed from our experimental results.
- While experiments were performed only for the vertical metal layers, the method is applicable to the horizontal metal layers also, keeping the vertical segments fixed.
- Almost all segments were assigned to a track by bipartite matching as described in Section 5. However, for some of the circuits we required Option (1) and Option (2) as mentioned in Section 5.2. Table 5 has the list of those circuits and the corresponding change in their wirelength in terms of pitch unit. The columns *Benchmark*, *Circuits*, *Opt*-1, *Opt*-2 and *WUnit* represents the name of the benchmark, the name of circuits, number of times Option (1) and Option (2) are used and the corresponding change in wirelength due to the inclusion of extra metal wire for connectivity.
- Since no information regarding delays of the circuits from the benchmarks were available to us, the delay before and after perturbation of the wire segments could not be compared. However, perturbations within the defined range values do not change the wirelength except only in a very few cases as given in Table 5 . Thus, change in the wirelength due to our perturbation method may not have a noticeable effect on the delay.
- The lower metal layers have more wires which provides more options to the wire perturbations. Hence, our results show better improvement for the lower metal layers than that for the higher ones.
- There is a notable reduction in dummy demand in the final layouts obtained by our proposed method thereby reducing metal costs for dummy fills along with other issues associated with them.
- Previous works [10, 13] have shown that the impact of dummification on reduction of flare is more compared to that by post-layout wire perturbation. Our proposed perturbation based method decreases flare with no additional overhead. Thus, in order to obtain further flare reduction, dummification can be applied as a post processing step of our perturbation method, which would definitely require less dummy fills than by dummification alone, and thereby reduce the layout cost and flare.
- In Ref. [19], a method has been reported to include dummification upto a user-specified bound simultaneously with wire perturbation, by which flare reduction obtained is more than that by wire perturbation alone. However, our results of the flow proposed here indicate that wire perturbation followed by dummification can yield better flare reduction.

TABLE 5 Change in wirelength due to track assignment

Benchmark	Circuit	Opt-1	Opt-2	WUnit
Faraday	DMA	2	3	2
	RISC1	-	4	-
	RISC2	1	1	2
ISPD′15	mgc_des_perf_1	3	2	4
	mgc_des_perf_b	2	1	2
	mgc_des_perf_a	2	1	3
	mgc_pci_bridge32_b	3	2	5

10 | CONCLUSION

To the best of our knowledge, this is the first study on minimisation of flare values by perturbation of wire segments at the post-layout stage using EUV lithography. A detailed study of perturbation-based method is performed using two types of target pattern density distribution models, namely Gaussian and sigmoidal. The results show significant minimisation of flare values for each of the benchmark suites. Moreover, we have also computed the dummy demand map before and after the wire perturbation which reflects reductions in dummy demand in the post-perturbed layouts. Both dummification and segment perturbations of highly optimised routed layout may introduce crosstalk. Hence, crosstalk aware perturbation and dummification needs to be done in the future for better circuit performance.

ACKNOWLEDGMENTS

The authors thank Prof. Shao-Yun Fang of National Taiwan University of Science and Technology for providing Benchmark suites for this work and sharing her valuable insight, and

also DST-GITA, and MoSPI, Government of India for the funding of this project.

ORCID

Sudipta Paul https://orcid.org/0000-0001-8699-5341
Susmita Sur-Kolay https://orcid.org/0000-0002-2052-3779

REFERENCES

1. Chen, H.Y., Chang, Y.W.: Routing for manufacturability and reliability. IEEE Circ. Syst. Mag. 9(3), 20–31 (2009)
2. Ghaida, R.S., et al.: A methodology for the early exploration of design rules for multiple-patterning technologies. In: Proceedings of the International Conference on Computer-Aided design, 50–56. ICCAD, San Jose (2012)
3. Kuang, J., Young, E.F.Y.: An efficient layout decomposition approach for triple patterning lithography. In: Proceedings of Design Automation Conference, 1–6, Austin, (2013)
4. Fang, S.Y., Chang, Y.W., Chen, W.Y.: A novel layout decomposition algorithm for triple patterning lithography. In: Proceedings of Design Automation Conference, 1181–1186. San Francisco (2012)
5. Chen, T., Liao, G., Chang, Y.W.: Predictive formulae for OPC with applications to lithography-friendly routing. IEEE Trans. Comput. Aided Des. Integr. Circ. Syst. 29(1), 40–50 (2010)
6. Park, S., et al.: Model based OPC for implant layer patterning considering wafer topography proximity (W3D) effects. In: Proceedings of SPIE, Optical Microlithography XXV, vol. 8326, pp. 237–243 (2012)
7. Huang, S.L., Lin, C.W., Chang, Y.W.: Efficient provably good OPC modeling and its applications to interconnect optimization. In: Proceedings of the International Conference on Computer Design, pp. 336–341. Amsterdam (2010)
8. Aoyama, H., et al.: Applicability of extreme ultraviolet lithography to fabrication of half pitch 35nm interconnects. In: Proceedings of SPIE, Extreme Ultraviolet (EUV) lithography, 7636, 566–577, San Jose (2010)
9. Wood, O., et al.: Integration of EUV lithography in the fabrication of 22-nm node devices. In: Proceedings of SPIE, Alternative Lithographic Technologies, 7271, 50–59 (2009)
10. Fang, S.Y., Chang, Y.W.: Simultaneous flare level and flare variation minimization with dummification in EUVL. In: Proceedings of Design Automation Conference, pp. 1179–1184. DAC, San Francisco (2012)
11. Lee, J., et al.: A study of flare variation in extreme ultraviolet lithography for sub-22 nm line and space pattern. Jpn. J. Appl. Phys. 49(6S), 06GD09 (2010)
12. Krautschik, C.G., et al.: Impact of EUV light scatter on CD control as a result of mask density changes. In: Proceedings of SPIE, Emerging Lithographic Technologies VI, 4688, 289–301. Santa Clara (2002)
13. Chiang, H.K., et al.: Simultaneous EUV flare variation minimization and CMP control by coupling-aware dummification. IEEE Trans. Comput. Aided Des. Integr. Circ. Syst. 35(4), 598–610 (2016)
14. Xiang, H., et al.: Fast dummy-fill density analysis with coupling constraints. IEEE Trans. Comput. Aided Des. Integr. Circ. Syst. 27(4), 633–642 (2008)
15. Chen, H.Y., Chou, S.J., Chang, Y.W.: Density gradient minimization with coupling-constrained dummy fill for cmp control. In: Proceedings of International Symposium on Physical Design, 105–111. ISPD, New York (2010)
16. Paul, S., Banerjee, P., Sur-Kolay, S.: Flare reduction in EUV lithography by perturbation of wire segments. In: Proceedings of International Conference on Very Large Scale Integration, Kolay, 7–12. VLSI-SoC, Daejeon (2015)
17. Schellenberg, F.M., Word, J., Toublan, O.: Layout compensation for EUV flare. In: Proceedings of SPIE, Emerging Lithographic Technologies IX, 5751, 320–329. San Jose (2005)
18. Zuniga, C., et al.: EUV flare and proximity modeling and model-based correction. In: Proceedings of SPIE, Extreme Ultraviolet (EUV) Lithography II, 7969, 262–274. San Jose (2011)
19. Paul, S., Banerjee, P., Sur-Kolay, S.: Minimization of flare in EUVL by simultaneous wire segment perturbation and dummification. In: Proceedings of IEEE Computer Society Annual Symposium on VLSI, 212–217. ISVLSI, Miami (2019)
20. Pan, S., Chang, Y.W.: Crosstalk-constrained performance optimization by using wire sizing and perturbation. In: Proceedings of International Conference on Computer Design, pp. 581–584. ICCD, Austin (2000)
21. 'lp-solve', http://lpsolve.sourceforge.net/5.5 Accessed 27 February 2021
22. Paul, S., Banerjee, P., Sur-Kolay, S.: Post-layout perturbation towards stitch friendly layout for multiple e-beam lithography. In: Proceedings of International Conference on Computer Design, Kolay, 411–414. ICCD, Boston (2017)
23. Stine, B.E., et al.: The physical and electrical effects of metal-fill patterning practices for oxide chemical-mechanical polishing processes. IEEE Trans. Electron. Dev. 45(3), 665–679 (1998)
24. Hopcroft, J.E., Karp, R.M.: An $n^{5/2}$ algorithm for maximum matchings in bipartite graphs. SIAM J. Comput. 2(4), 225–231 (1973)
25. 'Matlab': https://in.mathworks.com/products/matlab.html Accessed 27 February 2021
26. Networkx library: https://pypi.python.org/pypi/networkx Accessed 27 February 2021
27. Brglez, F., Bryan, D., Kozminski, K.: Combinational profiles of sequential benchmark circuits. In: Proceedings of International Symposium on Circuits and Systems (ISCAS), 3, 1929–1934. Portland (1989)
28. Kozminski, K.: Benchmarks for layout synthesis - evolution and current status. In: Proceedings of Design Automation Conference, 265–270. DAC, San Francisco (1991)
29. Adya, S.N., et al.: Unification of partitioning, placement and floorplanning. In: Proceedings of International Conference on Computer-Aided Design, 550–557. ICCAD, San Jose (2004)
30. Faraday: http://vlsicad.eecs.umich.edu/BK/ICCAD04bench Accessed 27 February 2021
31. Bustany, I.S., et al.: ISPD 2015 benchmarks with fence regions and routing blockages for detailed-routing-driven placement. In: Proceedings of International Symposium on Physical Design, 157–164. ISPD, New York (2015)

How to cite this article: Paul S, Banerjee P, Sur-Kolay S. A study on flare minimisation in EUV lithography by post-layout re-allocation of wire segments. *IET Circuits Devices Syst*. 2021;15:310–329. https://doi.org/10.1049/cds2.12028

APPENDIX I

Reduction in Flare

Table A1 shows the results of wire segment perturbation on all benchmark circuits using Gaussian and sigmoidal target density maps. Columns *Circuit* and *ML#* give the name of the circuit and the vertical metal layer on which wire segment perturbation is performed. The major Column *Initial* shows the flare values for the input layout. The major Columns *Our ILP-based method + track assignment* and *Relaxed ILP + track assignment* show the flare values for the final layout achieved by our proposed ILP, and ILP with constraints relaxation, respectively.

The minor columns labelled *Variation* and *Mean* under the three major columns show the corresponding values of flare variation and mean.

Columns *%Pert* and *Time* represent the percentage of the wire segments perturbed, and the execution times for *Initial*, *Our ILP-based method + track assignment* and *Relaxed ILP + track assignment*. Circuits in the same benchmark suite are grouped under the row header with the name of the benchmark suite. The layer wise improvement over all the circuits in a benchmark suite is computed using the geometric mean, and normalised with respect to initial values. The rows showing overall improvements for each benchmark suite are highlighted.

APPENDIX II

Reduction in Dummy Demand

Table A2 lists the reduction of post-perturbation dummy demand for MCNC, ISPD′15 and FARADAY benchmark circuits, respectively. The structure of the table is same as that of Table A1 . The minor columns named *variation* and *Mean* represent the variation of dummy demand and average dummy demand density. The columns *Circuit* and *ML#* and represent the name of the circuits and the vertical layer number. The major column *Initial* shows the total requirement of dummy fills in terms of density for the input layout. The columns named *Our ILP-based method + track assignment* and *Relaxed ILP + track assignment* report the dummy fill demand density in the final layout after perturbation using Gaussian and sigmoidal target density maps. In this table, layer wise overall improvement is similarly computed using geometric mean and normalised with respect to initial values. The overall improvement values are highlighted for every benchmark suites.

TABLE A1 Flare reduction results for MCNC, Faraday and ISPD′15 benchmark suites

		Initial		Using Gaussian Target Density Map								Using Sigmoidal Target Density Map							
				Our ILP-based method + track assignment				Relaxed ILP + track assignment				Our ILP-based method + track assignment				Relaxed ILP + track assignment			
Circuit	**ML#**	**Variation**	**Mean**	**Variation**	**Mean**	**%Pert**	**Time(s)**	**Variation**	**Mean**	**%Pert**	**Time(s)**	**Variation**	**Mean**	**%Pert**	**Time(s)**	**Variation**	**Mean**	**%Pert**	**Time(s)**
								MCNC Benchmark Circuits											
s13207	M2	0.2005	0.1921	0.1572	0.1799	58.23	25.78	0.1374	0.1730	70.02	10.56	0.1457	0.1723	62.30	28.88	0.1256	0.1690	76.67	11.23
s15850	M2	0.1998	0.1940	0.1741	0.1833	60.63	19.36	0.1699	0.1830	68.54	12.00	0.1623	0.1810	59.25	22.36	0.1586	0.1796	70.23	10.03
s38584	M2	0.2057	0.1938	0.1679	0.1791	63.39	35.95	0.1574	0.1799	76.33	15.20	0.1579	0.1689	64.21	30.55	0.1533	0.1703	78.03	13.00
s38417	M2	0.2083	0.1975	0.1775	0.1826	61.07	38.20	0.1695	0.1786	72.30	15.78	0.1747	0.1827	65.45	30.00	0.1638	0.1705	69.90	19.30
s5378	M2	0.2075	0.1972	0.1691	0.1802	52.90	21.23	0.1575	0.1835	68.84	09.10	0.1609	0.1855	56.64	13.93	0.1495	0.1800	65.58	07.83
s9234	M2	0.1960	0.2030	0.1690	0.1953	50.68	13.60	0.1560	0.1930	66.52	05.56	0.1706	0.1924	48.88	19.33	0.1469	0.1867	73.94	07.50
Struct	M2	0.2731	0.2596	0.2322	0.2432	48.95	13.86	0.2132	0.2396	67.12	07.33	0.2161	0.2390	43.93	12.57	0.1978	0.2262	68.84	10.20
primary1	M2	0.2743	0.2603	0.2309	0.2380	64.35	30.59	0.2251	0.2303	73.56	19.52	0.2265	0.2463	55.95	24.06	0.2030	0.2253	74.96	15.00
primary2	M2	0.2707	0.2565	0.2321	0.2370	57.60	39.16	0.2203	0.2265	75.47	20.47	0.2134	0.2340	61.39	34.78	0.1913	0.2185	77.72	17.63
Geomean	**M2**	**0.2239**	**0.2152**	**0.1877**	**0.2004**	**–**	**24.59**	**0.1760**	**0.1972**	**–**	**11.82**	**0.1788**	**0.1983**	**–**	**22.82**	**0.1637**	**0.1905**	**–**	**11.81**
Norm	**M2**	**1**	**1**	**0.84**	**0.93**	**–**	**1**	**0.79**	**0.92**	**–**	**0.48**	**0.80**	**0.92**	**–**	**1**	**0.73**	**0.89**	**–**	**0.52**
								FARADAY Benchmark Circuits											
	M2	0.1877	0.1756	0.1692	0.1648	49.10		0.1612	0.1584	62.20		0.14753	0.1577	56.30		0.1396	0.1510	78.02	
DMA	M4	0.1942	0.1934	0.1788	0.1864	30.80	463	0.1711	0.1843	46.38	335	0.1773	0.1833	43.10	549	0.1665	0.1801	55.50	409
	M6	0.2020	0.2066	0.1985	0.2042	23.95		0.1915	0.1993	35.25		0.1912	0.2022	40.98		0.1870	0.1960	53.92	
	M2	0.2228	0.1952	0.1907	0.1840	54.06		0.1793	0.1803	68.00		0.1750	0.1690	70.22		0.1627	0.1609	82.03	
DSP1	M4	0.2239	0.2030	0.2113	0.1989	43.20	737	0.2042	0.1953	51.09	488	0.1999	0.1901	39.20	711	0.1905	0.1838	60.93	416
	M6	0.2139	0.2030	0.2104	0.2011	20.30		0.2044	0.1970	38.18		0.2046	0.1969	47.50		0.2021	0.1966	37.80	
	M2	0.1971	0.1853	0.1544	0.1691	66.53		0.1488	0.1665	76.64		0.1491	0.1567	68.04		0.1420	0.1571	80.59	
DSP2	M4	0.1997	0.1948	0.1854	0.1861	39.02	694	0.1864	0.1865	60.68	493	0.1783	0.1819	44.76	693	0.1703	0.1807	56.73	450
	M6	0.2292	0.2228	0.2269	0.2214	34.00		0.2210	0.2174	29.09		0.2173	0.2154	19.44		0.2140	0.2127	33.03	
	M2	0.2439	0.2067	0.2075	0.1907	46.74		0.2051	0.1896	64.76		0.1992	0.1836	59.00		0.1923	0.1803	74.75	
RISC1	M4	0.2246	0.1978	0.2114	0.1898	32.37	1139	0.2062	0.1907	46.00	738	0.2053	0.1849	26.53	781	0.1968	0.1812	35.60	600
	M6	0.2417	0.2103	0.2390	0.2076	22.50		0.2350	0.2076	30.08		0.2350	0.2060	17.93		0.2251	0.2024	22.96	
	M2	0.2098	0.1988	0.1783	0.1803	42.60		0.1703	0.1782	66.28		0.1685	0.1762	62.00		0.1604	0.1717	76.30	

(Continues)

TABLE A1 (Continued)

		Initial		Using Gaussian Target Density Map								Using Sigmoidal Target Density Map							
				Our ILP-based method + track assignment				Relaxed ILP + track assignment				Our ILP-based method + track assignment				Relaxed ILP + track assignment			
Circuit	ML#	Variation	Mean	Variation	Mean	%Pert	Time(s)	Variation	Mean	%Pert	Time(s)	Variation	Mean	%Pert	Time(s)	Variation	Mean	%Pert	Time(s)
RISC2	M4	0.1843	0.1848	0.1719	0.1777	27.06	1065	0.1655	0.1772	42.57	723	0.1688	0.1746	33.25	728	0.1629	0.1701	51.33	499
	M6	0.2093	0.2046	0.2055	0.2024	19.95		0.2015	0.1994	29.07		0.2020	0.2003	21.00		0.1929	0.1963	26.12	
	M2	**0.2114**	**0.1920**	**0.1791**	**0.1775**	**–**		**0.1719**	**0.1743**	**–**		**0.1668**	**0.1683**	**–**		**0.1583**	**0.1639**	**–**	
Geomean	**M4**	**0.2047**	**0.1946**	**0.1911**	**0.1877**	**–**	**779.21**	**0.1859**	**0.1867**	**–**	**532.97**	**0.1854**	**0.1829**	**–**	**687.69**	**0.1769**	**0.1791**	**–**	**469.96**
	M6	**0.2188**	**0.2093**	**0.2156**	**0.2072**	**–**		**0.2101**	**0.2040**	**–**		**0.2095**	**0.2040**	**–**		**0.2038**	**0.2007**	**–**	
	M2	**1**	**1**	**0.85**	**0.93**	**–**		**0.81**	**0.91**	**–**		**0.79**	**0.88**	**–**		**0.75**	**0.85**	**–**	
Norm	**M4**	**1**	**1**	**0.93**	**0.96**	**–**	**1**	**0.91**	**0.96**	**–**	**0.68**	**0.91**	**0.94**	**–**	**1**	**0.86**	**0.92**	**–**	**0.68**
	M6	**1**	**1**	**0.98**	**0.99**	**–**		**0.96**	**0.98**	**–**		**0.95**	**0.97**	**–**		**0.93**	**0.96**	**–**	
ISPD'15 Benchmark Circuits																			
mgc_des	M2	0.1794	0.1737	0.1666	0.1669	32.09		0.1616	0.1645	59.19		0.1532	0.1495	41.96		0.1437	0.1480	60.83	
_perf_1	M4	0.1465	0.1180	0.1399	0.1148	46.23	637	0.1393	0.1139	66.12	377	0.1372	0.1130	55.00	490	0.1360	0.1136	71.88	353
mgc_des	M2	0.2038	0.2098	0.1856	0.1980	46.20		0.1853	0.1958	63.55		0.1557	0.1876	42.58		0.1450	0.1696	65.79	
_perf_a	M4	0.1801	0.1860	0.1716	0.1804	39.62	734	0.1709	0.1802	58.63	468	0.1671	0.1792	32.98	614	0.1655	0.1790	40.25	396
mgc_des	M2	0.1935	0.1850	0.1811	0.1805	50.39		0.1780	0.1793	53.07		0.1378	0.1574	39.00		0.1269	0.1483	58.42	
_perf_b	M4	0.1891	0.0894	0.1841	0.0872	28.72	814	0.1838	0.0870	36.12	494	0.1799	0.0852	32.98	682	0.1757	0.0846	40.25	523
mgc_edit	M2	0.1353	0.1324	0.1235	0.1240	62.19		0.1196	0.1226	68.70		0.1071	0.1171	64.40		0.1041	0.1159	73.33	
_dist_a	M4	0.1626	0.1026	0.1582	0.1001	25.85	918	0.1566	0.0995	32.96	615	0.1551	0.0994	32.92	694	0.1512	0.0989	38.88	523
	M2	0.2023	0.1817	0.1746	0.1643	63.33		0.1723	0.1635	75.25		0.1606	0.1619	76.50		0.1535	0.1580	81.84	
mgc_fft_1	M4	0.1063	0.0948	0.0999	0.0919	50.33	341	0.0966	0.0916	58.41	177	0.0994	0.0929	48.00	319	0.0993	0.0928	67.30	186
	M2	0.1953	0.1656	0.1634	0.1484	59.00		0.1623	0.1489	78.00		0.1598	0.1498	60.87		0.1511	0.1472	79.10	
mgc_fft_2	M4	0.1741	0.1051	0.1640	0.1004	43.00	308	0.1646	0.1011	55.09	152	0.1599	0.0988	54.80	268	0.1584	0.0978	67.15	152
	M2	0.2586	0.2314	0.2227	0.2174	55.69		0.2073	0.2027	73.08		0.2143	0.2080	70.77		0.1913	0.2036	82.65	
mgc_fft_a	M4	0.2745	0.2247	0.2651	0.2194	22.94	309	0.2647	0.2205	34.95	138	0.2517	0.2127	40.53	443	0.2502	0.2096	57.20	199
	M2	0.2526	0.2305	0.2037	0.2097	44.76		0.2022	0.2054	77.72		0.1984	0.2035	57.20		0.1874	0.1994	74.25	
mgc_fft_b	M4	0.2545	0.2276	0.2447	0.2205	27.66	280	0.2441	0.2211	39.78	126	0.2416	0.2197	24.70	266	0.2385	0.2187	43.84	116
mgc_pci_	M2	0.2431	0.1788	0.2146	0.1650	50.63		0.2131	0.1623	67.25		0.2032	0.1629	59.50		0.1908	0.1601	76.10	
bridge32_a	M4	0.1944	0.1247	0.1894	0.1223	29.05	238	0.1894	0.1223	46.00	134	0.1783	0.1196	34.88	272	0.1756	0.1186	53.15	156

TABLE A1 (Continued)

		Initial		Using Gaussian Target Density Map								Using Sigmoidal Target Density Map							
				Our ILP-based method + track assignment				Relaxed ILP + track assignment				Our ILP-based method + track assignment				Relaxed ILP + track assignment			
Circuit	**ML#**	**Variation**	**Mean**	**Variation**	**Mean**	**%Pert**	**Time(s)**	**Variation**	**Mean**	**%Pert**	**Time(s)**	**Variation**	**Mean**	**%Pert**	**Time(s)**	**Variation**	**Mean**	**%Pert**	**Time(s)**
mgc_pci_	M2	0.2468	0.2283	0.2142	0.2142	43.88		0.2139	0.2083	64.52		0.1926	0.2002	51.00		0.1817	0.1999	69.30	
bridge32_b	M4	0.2348	0.2206	0.2270	0.2161	53.80	217	0.2244	0.2160	38.62	186	0.2146	0.2122	44.70	218	0.2133	0.2096	57.00	179
	M2	**0.2075**	**0.1891**	**0.1826**	**0.1763**	**–**		**0.1792**	**0.1732**	**–**		**0.1651**	**0.1674**	**–**		**0.1549**	**0.1628**	**–**	
Geomean	**M4**	**0.1854**	**0.1396**	**0.1780**	**0.1358**	**–**	**418.29**	**0.1769**	**0.1357**	**–**	**239.66**	**0.1728**	**0.1340**	**–**	**391.72**	**0.1707**	**0.1332**	**–**	**242.28**
	M2	**1**	**1**	**0.88**	**0.93**	**–**	**–**	**0.86**	**0.92**	**–**	**–**	**0.79**	**0.88**	**–**	**–**	**0.75**	**0.86**	**–**	**–**
Norm	**M4**	**1**	**1**	**0.96**	**0.97**	**–**	**1**	**0.95**	**0.97**	**–**	**0.57**	**0.93**	**0.96**	**–**	**1**	**0.92**	**0.95**	**–**	**0.62**

TABLE A2 Reduction in Dummy Demand Density for MCNC, Faraday and ISPD′15 Benchmark suites

		Initial		Using Gaussian Target Density Map				Using Sigmoidal Target Density Map			
				Our ILP-based method + track assignment		Relaxed ILP + track assignment		Our ILP-based method + track assignment		Relaxed ILP + track assignment	
Circuit	ML#	Variation	Mean	Variation	Mean	Variation	Mean	Variation	Mean	Variation	Mean
						MCNC Benchmark Circuits					
s13207	M2	0.1717	0.1650	0.1399	0.1458	0.1362	0.1428	0.1170	0.1354	0.1110	0.1307
s15850	M2	0.1749	0.1666	0.1566	0.1573	0.1498	0.1512	0.1314	0.1454	0.1268	0.1395
s38584	M2	0.1743	0.1669	0.1468	0.1521	0.1399	0.1489	0.1372	0.1467	0.1340	0.1403
s38417	M2	0.1782	0.1699	0.1475	0.1499	0.1416	0.1471	0.1415	0.1496	0.1352	0.1431
s5378	M2	0.1793	0.1693	0.1524	0.1551	0.1419	0.1485	0.1350	0.1451	0.1224	0.1381
s9234	M2	0.1802	0.1738	0.1533	0.1566	0.1459	0.1541	0.1310	0.1408	0.1221	0.1402
Struct	M2	0.2311	0.2238	0.1940	0.2004	0.1883	0.2023	0.1558	0.1863	0.1501	0.1832
primary1	M2	0.2319	0.2243	0.1993	0.2081	0.1894	0.1993	0.1814	0.1953	0.1624	0.1850
primary2	M2	0.2287	0.2211	0.1927	0.1992	0.1869	0.1984	0.1742	0.1896	0.1539	0.1837
Geomean	**M2**	**0.1929**	**0.1851**	**0.1633**	**0.1678**	**0.1563**	**0.1642**	**0.1436**	**0.1579**	**0.1344**	**0.1523**
Norm	**M2**	**1**	**1**	**0.85**	**0.91**	**0.81**	**0.89**	**0.74**	**0.85**	**0.70**	**0.82**
						FARADAY Benchmark Circuits					
	M2	0.1570	0.1511	0.1341	0.1382	0.1260	0.1330	0.1108	0.1247	0.1040	0.1206
DMA	M4	0.1718	0.1659	0.1519	0.1568	0.1461	0.1518	0.1443	0.1514	0.1403	0.1505
	M6	0.1830	0.1770	0.1683	0.1706	0.1668	0.1694	0.1656	0.1674	0.1614	0.1630
	M2	0.1750	0.1619	0.1404	0.1425	0.1338	0.1368	0.1336	0.1353	0.1267	0.1341
DSP1	M4	0.1811	0.1681	0.1595	0.1567	0.1577	0.1559	0.1517	0.1523	0.1436	0.1479
	M6	0.2014	0.1869	0.1934	0.1850	0.1903	0.1838	0.1877	0.1808	0.1853	0.1795
	M2	0.1628	0.1534	0.1241	0.1299	0.1135	0.1268	0.1141	0.1260	0.1085	0.1234
DSP2	M4	0.1705	0.1611	0.1572	0.1545	0.1533	0.1531	0.1421	0.1435	0.1358	0.1409
	M6	0.1949	0.1843	0.1861	0.1804	0.1848	0.1799	0.1818	0.1781	0.1782	0.1739
	M2	0.1801	0.1637	0.1523	0.1500	0.1478	0.1433	0.1412	0.1372	0.1322	0.1347
RISC1	M4	0.1756	0.1608	0.1616	0.1538	0.1576	0.1499	0.1549	0.1497	0.1510	0.1480
	M6	0.1881	0.1711	0.1829	0.1677	0.1808	0.1673	0.1686	0.1616	0.1673	0.1600
	M2	0.1647	0.1538	0.1382	0.1390	0.1316	0.1348	0.1220	0.1303	0.1178	0.1253
RISC2	M4	0.1599	0.1493	0.1485	0.1410	0.1415	0.1400	0.1408	0.1379	0.1341	0.1351
	M6	0.1782	0.1654	0.1756	0.1637	0.1732	0.1640	0.1688	0.1606	0.1643	0.1591
	M2	**0.1677**	**0.1567**	**0.1375**	**0.1398**	**0.1300**	**0.1348**	**0.1238**	**0.1306**	**0.1174**	**0.1275**
Geomean	**M4**	**0.1716**	**0.1609**	**0.1559**	**0.1524**	**0.1511**	**0.1501**	**0.1467**	**0.1468**	**0.1408**	**0.1443**
	M6	**0.1889**	**0.1768**	**0.1811**	**0.1733**	**0.1790**	**0.1726**	**0.1743**	**0.1695**	**0.1711**	**0.1669**
	M2	**1**	**1**	**0.82**	**0.89**	**0.78**	**0.86**	**0.74**	**0.83**	**0.70**	**0.81**
Norm	**M4**	**1**	**1**	**0.91**	**0.95**	**0.88**	**0.93**	**0.85**	**0.91**	**0.82**	**0.90**
	M6	**1**	**1**	**0.96**	**0.98**	**0.95**	**0.98**	**0.92**	**0.96**	**0.91**	**0.94**
						ISPD′15 Benchmark Circuits					
mgc_des	M2	0.1490	0.1406	0.1309	0.1316	0.1241	0.1270	0.1220	0.1264	0.1160	0.1222
_perf_1	M4	0.1086	0.0944	0.1031	0.0916	0.1016	0.0912	0.1022	0.0907	0.1002	0.0899

TABLE A2 (Continued)

Circuit	ML#	Initial		Using Gaussian Target Density Map				Using Sigmoidal Target Density Map			
				Our ILP-based method + track assignment		Relaxed ILP + track assignment		Our ILP-based method + track assignment		Relaxed ILP + track assignment	
		Variation	Mean	Variation	Mean	Variation	Mean	Variation	Mean	Variation	Mean
mgc_des	M2	0.1804	0.1690	0.1612	0.1597	0.1558	0.1548	0.1507	0.1539	0.1487	0.1523
_perf_a	M4	0.1613	0.1489	0.1527	0.1449	0.1487	0.1441	0.1481	0.1422	0.1447	0.1414
mgc_des	M2	0.1594	0.1498	0.1441	0.1441	0.1434	0.1421	0.1377	0.1387	0.1335	0.1344
_perf_b	M4	0.1035	0.0703	0.0999	0.0689	0.0986	0.0681	0.0975	0.0677	0.0945	0.0662
mgc_edit	M2	0.1177	0.1061	0.1052	0.0988	0.1021	0.0987	0.0962	0.0943	0.0916	0.0912
_dist_a	M4	0.1046	0.0818	0.1010	0.0810	0.0997	0.0802	0.0991	0.0795	0.0975	0.0792
	M2	0.1587	0.1477	0.1329	0.1346	0.1265	0.1287	0.1246	0.1277	0.1214	0.1262
mgc_fft_1	M4	0.0995	0.0619	0.0948	0.0606	0.0935	0.0602	0.0943	0.0606	0.0932	0.0588
	M2	0.1473	0.1349	0.1162	0.1175	0.1113	0.1150	0.1168	0.1160	0.1141	0.1144
mgc_fft_2	M4	0.1147	0.0812	0.1094	0.0796	0.1085	0.0794	0.1070	0.0778	0.1067	0.0766
	M2	0.2015	0.1881	0.1622	0.1671	0.1532	0.1571	0.1487	0.1589	0.1441	0.1563
mgc_fft_a	M4	0.1999	0.1832	0.1928	0.1813	0.1897	0.1795	0.1827	0.1765	0.1786	0.1754
	M2	0.2001	0.1871	0.1627	0.1668	0.1529	0.1585	0.1546	0.1597	0.1497	0.1546
mgc_fft_b	M4	0.1989	0.1848	0.1881	0.1793	0.1876	0.1776	0.1855	0.1776	0.1851	0.1773
mgc_pci_	M2	0.1663	0.1463	0.1439	0.1347	0.1359	0.1294	0.1349	0.1303	0.1331	0.1300
bridge32_a	M4	0.1339	0.0801	0.1304	0.0785	0.1284	0.0779	0.1283	0.0778	0.1269	0.0770
mgc_pci_	M2	0.1997	0.1850	0.1641	0.1676	0.1570	0.1615	0.1536	0.1578	0.1529	0.1558
bridge32_b	M4	0.1942	0.1784	0.1862	0.1731	0.1837	0.1716	0.1849	0.1731	0.1809	0.1714
	M2	**0.1659**	**0.1533**	**0.1409**	**0.1404**	**0.1349**	**0.1357**	**0.1327**	**0.1347**	**0.1291**	**0.1320**
Geomean	**M4**	**0.1365**	**0.1070**	**0.1307**	**0.1047**	**0.1289**	**0.1039**	**0.1281**	**0.1033**	**0.1260**	**0.1021**
	M2	**1**	**1**	**0.85**	**0.92**	**0.81**	**0.89**	**0.80**	**0.88**	**0.78**	**0.86**
Norm	**M4**	**1**	**1**	**0.96**	**0.98**	**0.95**	**0.97**	**0.94**	**0.97**	**0.92**	**0.95**