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A comparison of random discrete dopant induced variability between Ge and Si junctionless p-FinFETs

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In this letter, the random discrete dopant (RDD) induced variability for a Ge junctionless (JL) p-FinFET is reported. A one-to-one comparison of the RDD-induced variability between Ge and Si JL FinFETs for varying device parameters and supply voltage is made using a 3-D numerical device simulator. Results indicate that the Ge JL FinFET shows higher immunity to RDD induced threshold voltage fluctuation than its Si counterpart, which is partially due to the higher dielectric constant of Ge than Si. Because of the lower band gap of Ge than Si, a higher variation in subthreshold swing due to RDD is, however, observed for Ge devices. Technology scaling is found to reduce σSS, although it has almost no effects on σV_T for both types of devices. The difference in σSS between Ge and Si devices decreases with technology scaling, which makes Ge very attractive for scaled p-type JL FinFETs. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4927279]

Further downscaling of device dimensions for conventional metal-oxide-semiconductor field-effect transistor (MOSFET) poses a great challenge due to the need of ultra-steep source/drain doping profiles. A junctionless transistor (JLT),[1] which does not require such doping profiles, has been proved to be a promising candidate for future technology nodes. Such a device offers some advantages over its conventional counterpart. These include simple fabrication process due to the absence of source drain junctions, better short channel immunity and, hence, better scalability, good mobility at short gate lengths, steep subthreshold swing (SS) at relatively low drain bias due to impact ionization effect,[2] and low electric field in the ON-state.[3]

To meet with the industry requirements, such as high drive current and low gate delay, germanium shows promise as a future channel material, particularly for p-channel devices, owing to its higher bulk carrier mobility and compatibility with Si process line. Excellent I_{ON}/I_{OFF} performance,[4] high drain current,[5] and impressive short channel effect (SCE) control[6] have been demonstrated for germanium on insulator (GeOI) p-MOSFET. Recently, JLT on GeOI have been investigated[7–9] to combine the intrinsic properties of Ge with the excellent features of JLT.

The significance of random variability in transistor increases with the down-scaling of device dimensions, particularly for the sub-30-nm gate lengths, as it poses a great challenge in achieving high yield in integrated circuit manufacturing. Random discrete dopant (RDD), gate line-edge roughness, and gate metal work-function induced variability are the serious issues for conventional MOSFET.[10] In a JLT, there are no p-n junctions. The channel doping concentration and type for such a device are the same as those for the source and drain regions. For this reason, the channel doping in the case of a JL device is henceforth referred to not only the doping of the channel region but also the doping of the source and drain regions. High channel doping concentration ($\sim 10^{19}\,cm^{-3}$) is generally required for proper operation of a JL FinFET that is in contrast with the case of a conventional FinFET for which an intrinsic channel is used. Owing to such high channel doping, RDD has been identified as the major source of variability for junctionless devices.[11,12] The impact of RDD induced variability on Ge JLT is still unexplored. In this letter, we report the impact of RDD on Ge JL p-FinFET and the results are compared with that of a similarly sized Si JL p-FinFET. It is shown that RDD induced threshold voltage V_T variation is significantly lower in Ge devices than Si devices, which is partially due to the higher dielectric constant of Ge than Si. On the other hand, higher leakage current arising out of the lower band gap of Ge results in higher RDD induced SS variation in the Ge devices than their Si counterparts.

The device structure of the p-channel JL FinFET, used in this study, is shown in Fig. 1(a). A buried oxide thickness T_{BOX} of 10 nm and an equivalent oxide thickness (EOT) of 0.8 nm for the gate dielectric are used for all the devices used in this study. All device dimensions and parameters except the value of the work function of the gate metal, which has been adjusted to achieve similar values of V_T, are kept similar for both Si and Ge devices.

To incorporate and analyze the effects of RDD, Sentaurus 3D numerical device simulator,[13] version H-2013.03, has been used. Randomization of doping profile for both types of JL FinFETs has been accomplished following the Sano's method[14] with a suitable value of screening factor k_c chosen according to the equation $k_c \approx 2(N_{D/A})^{1/3}$ where $N_{D/A}$ represents donor/acceptor concentration. In each case, we have simulated 200 devices with different randomized doping profiles. Such a randomized profile for JL FinFET is shown in Fig. 1(b).

Doping dependent (Masseti) and normal field dependent mobility models have been included in our device simulations. Quantum density gradient, Hurkx band-to-band tunneling, and band gap narrowing models are also activated. We have separately calibrated the simulation setup for the Ge and Si JL FinFETs with their experimental results, as reported in Refs. 9 and 15, respectively. A good agreement

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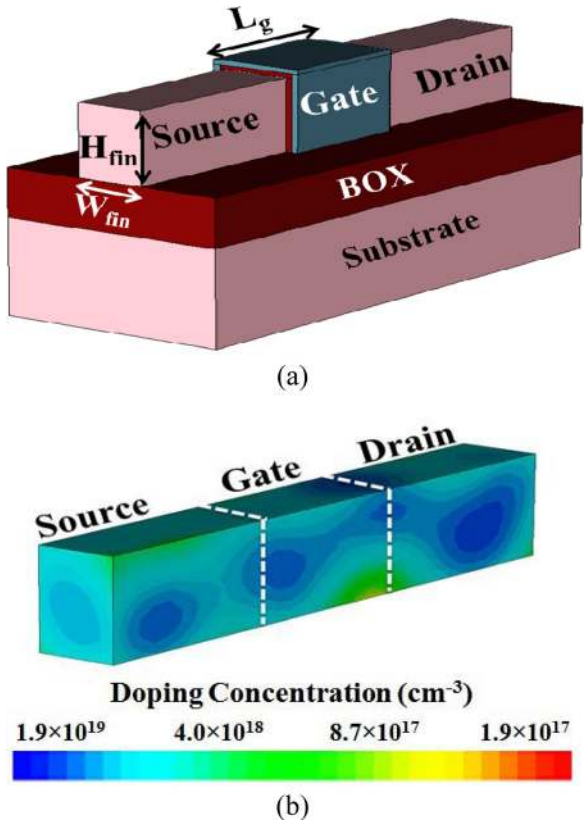

FIG. 1. (a) Schematic device structure and (b) randomized doping profile for JL FinFET.

between experimental and simulated characteristics can be visualized in Fig. 2 for both types of devices. It may be noted that since the value of D_{it} has not been reported for the Ge device in Ref. 9, a value of $3 \times 10^{12}\,cm^{-2}\,eV^{-1}$ is assumed for model calibration that resulted in a good fit.

Effects of RDD on the variability performance of both Ge and Si JL FinFETs have been considered by comparing numerical values of standard deviation of V_T (σV_T) and subthreshold swing SS (σSS), extracted from transfer characteristics. In order to also capture the impact of variation in different device parameters and supply voltage on the variability performance, we first perform simulations for

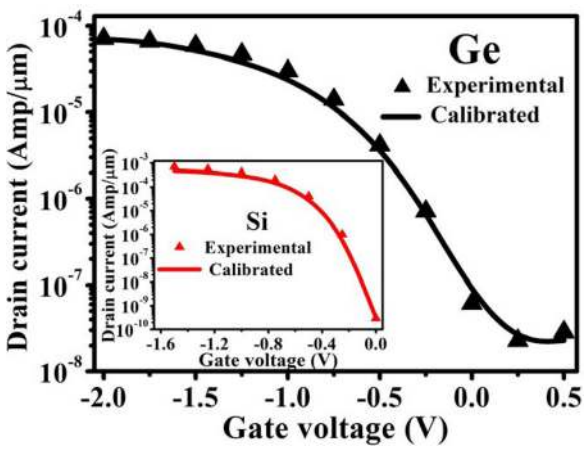

FIG. 2. Calibration of the model for Ge JL FinFET against the experimental data in Ref. 9. Inset shows the calibration of Si JL FinFET with the experimental data in Ref. 15.

different values of the gate length L_g, fin width W_{fin}, interface trap density D_{it}, channel doping concentration N_D, and supply voltage V_{DD} by varying one of them at a time. To make a comparison of the RDD induced variability between Ge and Si JL FinFETs for future technology nodes, simulations are then performed by simultaneously scaling different device parameters and V_{DD} relevant to such nodes. Results of both of them are summarized in Table I. It can be clearly seen in Table I that σV_T is significantly higher for the Si device than its Ge counterpart for all different combinations of the structural parameters. This can also be verified from the frequency distribution plot of V_T for a particular device, as shown in Fig. 3. The relatively higher immunity to the RDD induced V_T fluctuation of Ge devices than Si devices may partially be attributed to the higher fin capacitance arising out of the higher dielectric constant of Ge than Si, as can be predicted by the model in Ref. 16. It, however, fails to fully explain the enhanced immunity for Ge devices for which future investigations may be necessary.

Because of the higher dielectric constant of Ge, the nominal value of SS is found to be higher for the Ge JL FinFET than its Si counterpart, as can be seen in Table I, which is consistent with the previous report.[17] Higher values of σSS are also observed in Table I for Ge devices than Si devices for different combinations of the structural parameters. To explain it, simulations are performed for a Ge device without the BTBT model. It is clearly observed that when BTBT model is not included in the simulation, σSS for the Ge device becomes comparable to that for the Si device. Higher leakage current because of the lower band gap of Ge may, therefore, be attributed to higher σSS for Ge devices. Although not shown in Table I, it has been verified that inclusion or exclusion of the BTBT model in the simulation has almost no effects on either σV_T or σSS for Si devices. Slightly higher value of σSS for the Ge device than the Si device, when the BTBT model is not activated, may be attributed to higher short-channel effects in such devices arising out of the higher dielectric constant of Ge than Si.

It is also observed in Table I that a variation in D_{it} has almost no effects on relative results in terms of either σV_T or σSS between two types of devices. Since SCEs may be considered minimal for a device with $L_g > 5 \times W_{fin}$, a device with $L_g = 50\,nm$ and $W_{fin} = 8\,nm$ is also considered to see the impact of SCEs on the variability performance. Since the trend of the results do not change for this device in comparison with other devices, it may be concluded that SCEs also have almost no effects on either lower σV_T or higher σSS in Ge devices than Si devices.

It is also evident in Table I that both σV_T and σSS increase with L_g scaling, while they are reduced with W_{fin} scaling for both types of devices. This may be attributed to the increased and decreased short-channel effects with the scaling of L_g and W_{fin}, respectively.[18] As RDD induced variability is directly related to the number of dopant within the channel, both σV_T and σSS decrease with a decrease in the channel doping for both types of devices, as observed in Table I. Also, a reduction in V_{DD} from 1.0 to 0.8 V results in slightly reduced impact of RDD induced variability for both types of devices.

TABLE I. Standard deviation and mean values of threshold voltage and subthreshold swing.

Parameters							Ge				Si			
L_g (nm)	W_{fin} (nm)	H_{fin} (nm)	N_D (cm^{-3})	D_{it} ($cm^{-2}eV^{-1}$)	V_{DS} (V)	*BTBT*	*Mean* V_T (V)	σV_T (mV)	*Mean SS* (mV/dec)	σSS (mV/dec)	*Mean* V_T (V)	σV_T (mV)	*Mean SS* (mV/dec)	σSS (mV/dec)
20	08	15	1×10^{19}	1×10^{11}	−1.00	Yes	−0.19	42.51	91.60	5.68	−0.17	56.86	69.74	2.64
20	10	15	1×10^{19}	1×10^{11}	−1.00	Yes	−0.28	46.31	103.22	7.16	−0.27	65.36	74.07	3.47
30	08	15	1×10^{19}	1×10^{11}	−1.00	Yes	−0.26	31.67	91.20	4.71	−0.25	44.29	68.72	2.28
50	08	15	1×10^{19}	1×10^{11}	−1.00	Yes	−0.31	21.05	89.36	3.48	−0.30	32.84	68.04	2.01
20	08	15	1×10^{19}	1×10^{12}	−1.00	Yes	−0.21	43.03	90.57	5.83	−0.20	56.59	70.87	2.84
20	08	15	8×10^{18}	1×10^{11}	−1.00	Yes	−0.22	36.17	87.77	3.77	−0.21	51.57	70.71	2.21
20	08	15	1×10^{19}	1×10^{11}	−0.80	Yes	−0.18	40.75	89.70	4.94	−0.16	54.95	69.90	2.33
20	08	15	1×10^{19}	1×10^{11}	−1.00	No	−0.19	42.16	87.54	3.13	…	…	…	…
20	10	30	1×10^{19}	1×10^{11}	−0.81	Yes	−0.22	38.71	108.41	4.11	−0.21	50.36	73.51	2.30
15	07	25	1×10^{19}	1×10^{11}	−0.78	Yes	−0.23	38.53	94.11	2.88	−0.22	50.14	72.18	2.06
10	05	20	1×10^{19}	1×10^{11}	−0.66	Yes	−0.24	38.36	88.37	2.61	−0.22	49.86	72.08	1.74

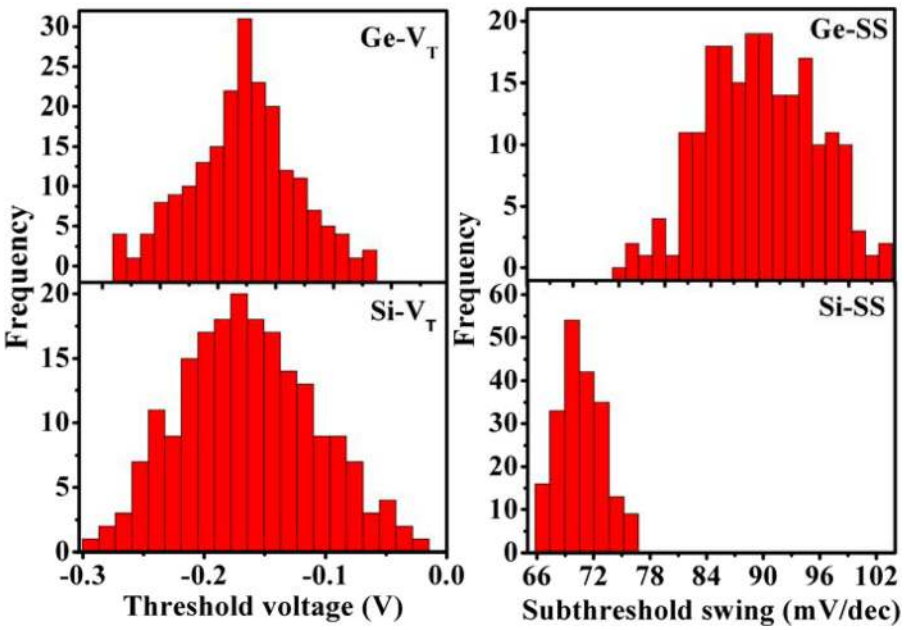

FIG. 3. Histograms for threshold voltage and subthreshold swing due to RDD for $L_g = 20$ nm, $W_{fin} = 8$ nm, $H_{fin} = 15$ nm, $N_D = 1\times10^{19}\,cm^{-3}$, and $D_{it} = 1\times10^{11}\,cm^{-2}eV^{-1}$ at $V_{DS} = 1.0$ V.

Since Pelgrom plot[19] is widely used to benchmark variability, we have plotted the correlation between σV_T and channel area in Fig. 4. A higher value of A_{vt}, which is defined by the slope of σV_T versus $1/\sqrt{(L_g \times W_{eff})}$ plot, is observed for Si JL FinFETs, which signifies higher variation in Si than Ge with progressive technology nodes.

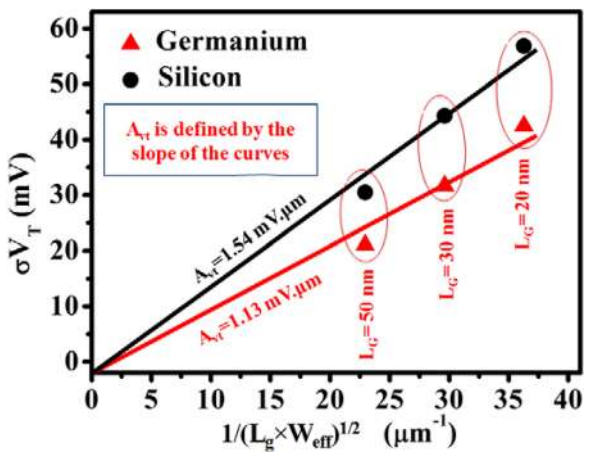

FIG. 4. Pelgrom plot for Ge and Si JL FinFETs.

Results of technology scaling following ITRS[20] roadmap, as shown in the last three rows in Table I, reveal the following. First, σSS is considerably reduced with technology scaling, although it has almost no effects on σV_T for both types of devices. This can be explained as follows. It is observed in Table I that the impact of L_g scaling, which degrades variability performance, is much higher on σV_T than σSS. On the other hand, the impact of W_{fin} scaling, which improves variability performance, is higher on σSS than σV_T. The trend of the results of H_{fin} scaling has been reported to be similar to that of L_g scaling.[12] As a result, when the technology is scaled, i.e., when all device dimensions are scaled, the combined degradation arising out of L_g and H_{fin} scaling is more or less compensated by the improvement due to W_{fin} scaling in the case of σV_T. On the other hand, the improvement arising out of the W_{fin} scaling is considerably higher than the combined degradation due to L_g and H_{fin} scaling in the case of σSS resulting in its improvement with technology scaling. Power supply scaling may

also have a role in the improvement in σSS with technology scaling. Second, σV_T is significantly ($\sim$25%) lower in Ge devices than Si devices for all technology nodes. Finally, the difference in σSS between Ge and Si devices decreases with technology scaling, which makes scaled Ge devices even more attractive than Si devices.

In summary, we made a one-to-one comparison of the RDD induced variability between Ge and Si JL p-FinFETs for varying device parameters and supply voltage. It has been found that a Ge JL FinFET is significantly less affected due to RDD induced V_T variability than its Si counterpart partially due to the higher dielectric constant of Ge than Si. The impact of RDD on SS is, however, much higher for the Ge JL FinFET mainly due to higher leakage currents in such devices arising out of the lower band gap of Ge than Si. Technology scaling reduces σSS, although it has almost no effects on σV_T for both types of devices. Also, the reduction in σSS is much higher for Ge devices than Si devices making Ge as an attractive channel material for p-type JL devices than Si particularly for scaled device dimensions.

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