

# A Synthesis Method for Quaternary Quantum Logic Circuits

Sudhindu Bikash Mandal<sup>1</sup>    Amlan Chakrabarti<sup>1</sup>    Susmita Sur-Kolay<sup>2</sup>

<sup>1</sup> A. K. Choudhury School of Information Technology, University of Calcutta, India

<sup>2</sup> Advanced Computing and Microelectronics Unit, Indian Statistical Institute, India

**Abstract.** Synthesis of quaternary quantum circuits involves basic quaternary gates and logic operations in the quaternary quantum domain. In this paper, we propose new projection operations and quaternary logic gates for synthesizing quaternary logic functions. We also demonstrate the realization of the proposed gates using basic quantum quaternary operations. We then employ our synthesis method to design of quaternary adder and some benchmark circuits. Our results in terms of circuit cost, are better than the existing works.

**Keywords:** Quaternary algebra, Quaternary quantum logic gates, Quaternary logic synthesis, Quaternary adder

## 1 Introduction

Quaternary quantum computing is gaining importance in the field of quantum information theory and quantum cryptography as it can represent a Galois Field(4) quantum system by the basis states  $|0\rangle$ ,  $|1\rangle$ ,  $|2\rangle$  and  $|3\rangle$ . The unit of information is called a *qudit* which is characterized by a wave function  $|\psi\rangle$  [1,2] expressed as a linear superposition of basis states. Multi-valued quantum algebra comprises the rules for a set of basic logic operations that can be performed on qudits. While in [3] the structure of a multi-valued logic gate is proposed which is experimentally feasible with a linear ion trap scheme for quantum computing; this approach can produce large dimensional circuits. A universal architecture for multi-valued reversible logic is given in [4], but quantum realization of the circuits thus obtained is not apparent. The universality of  $n$ -qudit gates is presented in [5], but no algorithms for synthesis were given. Al-Rabedi et al. proposed in [6] the minimization technique for multi-valued quantum Galois field sum of products (QGFSOP). Quaternary logic is one of the promising multi-valued quantum logic systems. The binary logic functions can be expressed by grouping 2-bits together into equivalent quaternary value [7]. This theoretically reduces the total volume of the physical devices needed to approximately  $1/\log_2^4$ , i.e.  $1/2$  the volume needed for binary system [7].

The realization of a given quaternary quantum function as a quantum circuit requires a set of gates for the quaternary logic operations. In [8], the realization of quaternary Feynman and Toffoli gates using 1-qudit and 2-qudit quaternary Muthukrishnan-Stroud gates (M-S Gate)[3] are illustrated. The QGFSOP expressions can be realized by using these Feynman and Toffoli gates [8]. The

method of synthesizing incompletely specified multi-output quaternary function using quaternary 1-qudit gates and multi-qudit controlled gates has been proposed in [9]. But this synthesis method is not applicable for any arbitrary quaternary functions. In [10], a heuristic algorithm is proposed for minimization of a QGFSOP expression for multi-output quaternary logic functions using a Quaternary Galois Field Decision Diagram (QGFDD). But no quantum gate level implementation was provided. In this paper, our specific contributions are as follows:

- new projection operation for synthesizing quaternary logic functions;
- new quaternary logic gates, namely Generalized Quaternary Gate (*GQG*), permutative quaternary Controlled Cyclic Shift gate (*C<sup>2</sup>CS*) and Modulo4 addition gate;
- new simplification rules for reduction in gate count and circuit levels for multivalued quantum circuits.

The rest of the paper is organized as follows. We provide the preliminary concepts of multivalued quantum computing in section 1. We propose the quaternary algebra with a new projection operation in section 2. In section 3, we introduce some new quaternary logic gates. The proposed synthesis methodology along with its simplification rules are presented in section 4. The synthesis results for some example circuits and their comparison with related work are given in section 5. Concluding remarks appear in section 6.

## 2 Quaternary Algebra

A brief summary of the quaternary addition, multiplication and NOT operations as well as the quaternary projection operations  $L$ ,  $J$  and (the new one)  $P$  are presented next. .

### 2.1 GF(4) arithmetic

Quaternary Galois field GF(4) is an algebraic structure consisting the set of elements  $Q=\{0, 1, 2, 3\}$ . The addition (+) and multiplication (.) operations over GF(4) are shown in the Table 1.

**Table 1.** GF(4) Addition and Multiplication

+	0	1	2	3	.	0	1	2	3
0	0	1	2	3	0	0	0	0	0
1	1	0	3	2	1	0	1	2	3
2	2	3	0	1	2	0	2	3	1
3	3	2	1	0	3	0	3	1	2

### 2.2 Quaternary Logical NOT

The logical NOT in quaternary quantum system is defined as  $NOT(a) = a + 1$ , where '+' denotes the modulo 4 addition, and  $a = \{0, 1, 2, 3\}$ .

### 2.3 Quaternary Projection Operations $L$ , $J$ and $P$

We present nine projection operations, grouped into three types  $L_i$ ,  $J_i$ , and  $P_i$ , where  $i = \{0, 1, 2, 3\}$ . While  $L_i$  and  $J_i$  types were defined earlier [11,12] as

$$L_i(a) = 1 \text{ if } a = i \text{ and } 0 \text{ otherwise, and}$$

$J_i(a) = 2$  if  $a = i$  and 0 otherwise.

We introduce the new  $P_i$  type operations, which are defined as

$P_i(a) = 3$  if  $a = i$  and  $a = 0$  otherwise.

Table 2 presents the truth tables for  $L_i, J_i,$  and  $P_i$  types of operators as well as for the derived operators  $L'_i, J'_i$  and  $P'_i$ . The  $L_i, J_i$  and  $P_i$  operations are commutative, associative and distributive over AND and OR logic.

**Table 2.** Truth table of projection operations  $L_i, L'_i, J_i, J'_i, P_i, P'_i$

$a$	0	1	2	3	$a$	0	1	2	3	$a$	0	1	2	3	$a$	0	1	2	3
$L_0(a)$	1	0	0	0	$J_2(a)$	0	0	2	0	$L'_0(a)$	0	1	1	1	$J'_2(a)$	2	2	0	2
$L_1(a)$	0	1	0	0	$J_3(a)$	0	0	0	2	$L'_1(a)$	1	0	1	1	$J'_3(a)$	2	2	2	0
$L_2(a)$	0	0	1	0	$P_0(a)$	3	0	0	0	$L'_2(a)$	1	1	0	1	$P'_0(a)$	0	3	3	3
$L_3(a)$	0	0	0	1	$P_1(a)$	0	3	0	0	$L'_3(a)$	1	1	1	0	$P'_1(a)$	3	0	3	3
$J_0(a)$	2	0	0	0	$P_2(a)$	0	0	3	0	$J'_0(a)$	0	2	2	2	$P'_2(a)$	3	3	0	3
$J_1(a)$	0	2	0	0	$P_3(a)$	0	0	0	3	$J'_1(a)$	2	0	2	2	$P'_3(a)$	3	3	3	0

### 3 Quaternary Logic Gates

The definitions of the existing quaternary logic gates as well as a few newly introduced quaternary logic gates are provided below. We also show the implementation of the newly proposed gates using basic quantum ternary operations.

#### 3.1 Quaternary Feynman, Quaternary Toffoli, MAX and MIN gates

The 2-qudit Quaternary Feynman gate [8] is defined as:

Feynman( $A, B$ ) =  $A + B$ , where '+' operator is addition over GF(4)(Figure 1.a).

The quaternary 3-qudit Toffoli gate [8], shown in Figure 1.b is defined as:

Toffoli( $A, B, C$ ) =  $A.B + C$ , where  $A$  and  $B$  are the control inputs and  $C$  the target input, '+' and '.' operators are addition and multiplication over GF(4). We use the quaternary MAX and MIN gates [13] respectively to replace the OR and the AND gates. These two gates are defined as

$$\text{MAX}(A_1, A_2, \dots, A_n, B) = \begin{cases} A_i & \text{if } A_i \geq A_j, i \neq j \text{ and } A_i \geq B; \\ B & \text{if } \forall i, B \geq A_i; \end{cases}$$

$$\text{MIN}(A_1, A_2, \dots, A_n, B) = \begin{cases} A_i & \text{if } A_i \leq A_j, i \neq j \text{ and } A_i \leq B; \\ B & \text{if } \forall i, B \leq A_i; \end{cases}$$

where  $i = \{1, 2, 3 \dots n\}$  (Figures 2.a, 2.b). The quaternary Feynman and Toffoli gates can be realized using quaternary M-S gates [7,8], defined as (Figure 2.c)

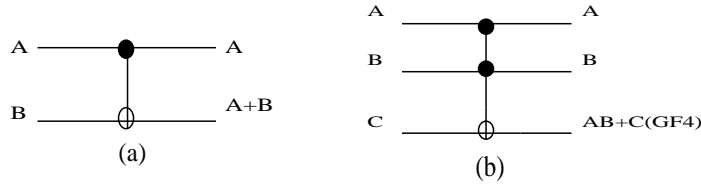
M-S( $A, B$ ) =  $Z$  operation on  $B$  if  $A = 3$ , otherwise  $B$ , where  $Z$  is one of the 24 shift operations [10] shown in Table 3.

#### 3.2 Generalized Quaternary Gate

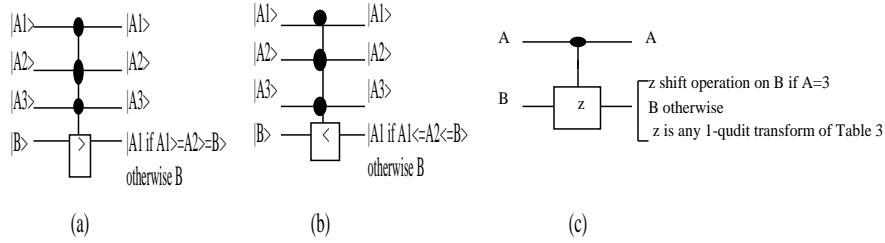
A new generalized quaternary gate (GQG) is required to realize the 24 shift operations [10] given in the Table 3. It is a multi-qudit gate shown in Figure 3.a. The controlling input of GQG can be used to select the 1-qudit shift operation on the target input. The GQG is formally defined as

**Table 3.** Shift Operations over GF(4) [10]

Symbol	Operation	Symbol	Operation	Symbol	Operation	Symbol	Operation
$x^{+0}$	$x = x$	$x^{021}$	$x = 2x + 2$	$x^{23}$	$x = x^2$	$x^{0231}$	$x = 2x^2 + 2$
$x^{+1}$	$x = x + 1$	$x^{032}$	$x = 2x + 3$	$x^{01}$	$x = x^2 + 1$	$x^{03}$	$x = 2x^2 + 3$
$x^{+2}$	$x = x + 2$	$x^{132}$	$x = 3x$	$x^{0213}$	$x = x^2 + 2$	$x^{13}$	$x = 3x^2$
$x^{+3}$	$x = x + 3$	$x^{012}$	$x = 3x + 1$	$x^{0312}$	$x = x^2 + 3$	$x^{0123}$	$x = 3x^2 + 1$
$x^{123}$	$x = 2x$	$x^{023}$	$x = 3x + 2$	$x^{12}$	$x = 2x^2$	$x^{02}$	$x = 3x^2 + 2$
$x^{013}$	$x = 2x + 1$	$x^{031}$	$x = 3x + 3$	$x^{0132}$	$x = 2x^2 + 1$	$x^{0321}$	$x = 3x^2 + 3$



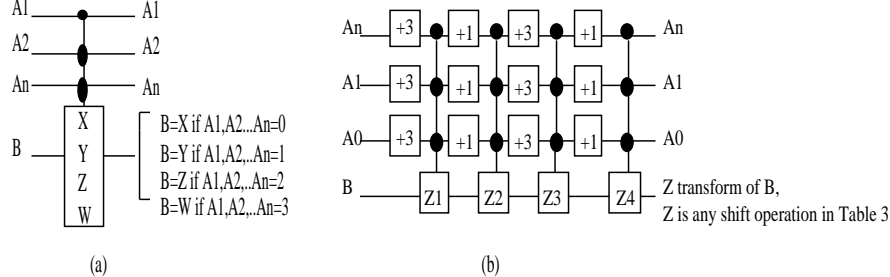
**Fig. 1.** (a) 2-qudit Quaternary Feynman gate (b) 3-qudit quaternary Toffoli gate



**Fig. 2.** (a) Quaternary MAX gate, (b) Quaternary MIN gate, (c) Quaternary M-S gate

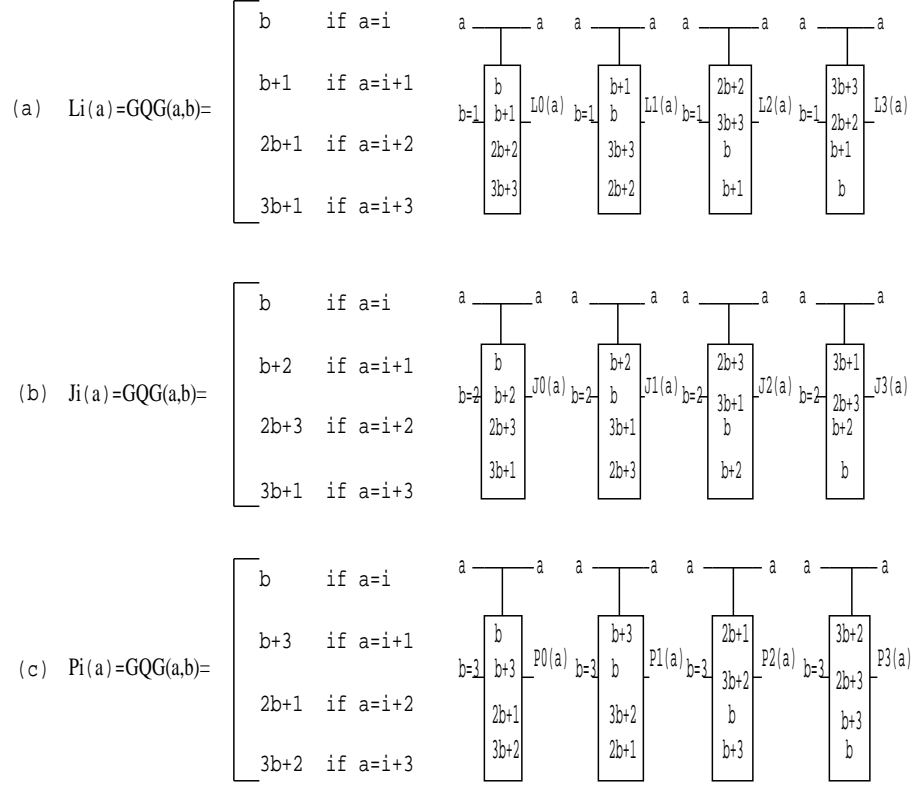
$$GQG(A_1, A_2, \dots, A_n, B) = \begin{cases} B \text{ shift } X & \text{if } A_1, A_2, \dots, A_n = 0; \\ B \text{ shift } Y & \text{if } A_1, A_2, \dots, A_n = 1; \\ B \text{ shift } Z & \text{if } A_1, A_2, \dots, A_n = 2; \\ B \text{ shift } W & \text{if } A_1, A_2, \dots, A_n = 3; \\ B & \text{otherwise;} \end{cases}$$

The realization of a GQG gate using quaternary M-S gates, is shown in Figure 3.b.



**Fig. 3.** (a) A multi-qudit generalized quaternary gate (GQG), and (b) its realization using M-S gates

**Implementation of  $L_i$ ,  $J_i$  and  $P_i$  operations using GQG** We can implement the  $L_i$ ,  $J_i$  and  $P_i$  operations by using a GQG, as shown in Figures 4.a, 4.b and 4.c respectively. For  $L_i$ ,  $J_i$  and  $P_i$  type operations, we set  $GQG(a,1)$ ,  $GQG(a,2)$  and  $GQG(a,3)$  respectively.



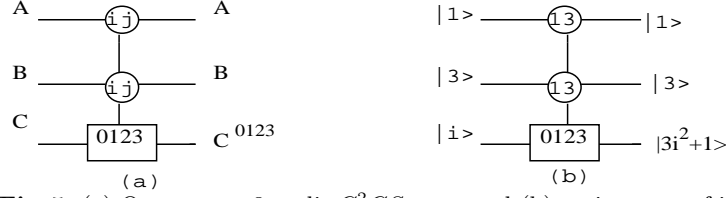
**Fig. 4.** GQG based realization of quaternary projection operations: (a) $L_i$ , (b) $J_i$  and (c) $P_i$

### 3.3 Quaternary Controlled Cyclic Shift $C^2CS$ gate

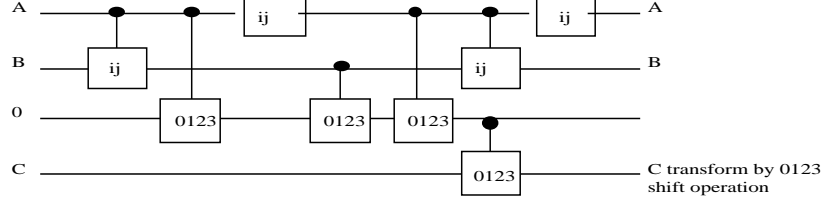
We propose a new 3-qudit  $C^2CS$  gate, used for realizing the simplification rules for quaternary minterms, as

$$C^2CS(A, B, C) = \begin{cases} C^{0123} & \text{if } A \neq B; \\ C & \text{otherwise;} \end{cases} \text{ where the values of the inputs are from}$$

the set  $\{1, 2, 3\}$  and  $C^{0123}$  is the cyclic shift operation  $x^{0123}$  defined in Table 3. The symbolic representation of  $C^2CS$  is shown in Figure 5.a and an instance of this gate is shown in Figure 5.b, where  $x^{0123}$  shift operation is applied on  $C$  if  $A = 1, B = 3$  or  $A = 3, B = 1$ . The realization of the  $C^2CS$  gate using M-S gates is shown in Figure 6.



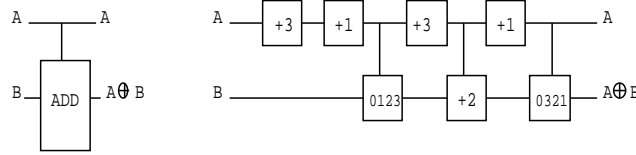
**Fig. 5.** (a) Quaternary 3-qudit  $C^2CS$  gate, and (b) an instance of it.



**Fig. 6.** Realization of quaternary 3-qudit  $C^2CS$  gate with M-S gates

### 3.4 A new Modulo4 Addition Gate

We introduce the new 2-qudit quaternary Modulo4 Addition gate as:  $\text{ADD}(A, B) = A \oplus B$ , where  $\oplus$  represent the modulo 4 addition. This gate can be used as a template for simplification of adder circuits. The symbolic representation of ADD gate is shown in Figure 7.a and the realization using quaternary M-S gate is shown in Figure 7.b



**Fig. 7.** (a) 2-qudit Modulo4 Addition Gate, and (b) its realization with M-S gates

## 4 Proposed Synthesis Methodology

### 4.1 Overview

Consider an  $m$ -variable quaternary quantum logic function

$$f(a_1, a_2, \dots, a_m) = \sum_{i=0}^n (\text{minterms for one})_i + \sum_{j=0}^p (\text{minterms for two})_j + \sum_{k=0}^s (\text{minterms for three})_k,$$

where  $\sum$  implies logical quaternary OR,  $n$ ,  $p$  and  $s$  are respectively the number of input vectors for which  $f$  is 1, 2 and 3. Thus,  $f$  is 0 for  $(4^m - n - p - s)$  of the input vectors. We express the minterms for *one*, *two* and *three* using the  $L_i$ ,  $J_i$  and  $P_i$  operations respectively. From Table II, we can state that

$$\prod_{i=1}^m L_0(a_i) = \begin{cases} 1 & \text{if } \forall i \ a_i = 0; \\ 0 & \text{if } \exists i \ a_i = 1, 2 \text{ or } 3; \end{cases} \quad \prod_{i=1}^m L_1(a_i) = \begin{cases} 1 & \text{if } \forall i \ a_i = 1; \\ 0 & \text{if } \exists i \ a_i = 0, 2 \text{ or } 3; \end{cases}$$

$$\prod_{i=1}^m L_2(a_i) = \begin{cases} 1 & \text{if } \forall i \ a_i = 2; \\ 0 & \text{if } \exists i \ a_i = 0, 1 \text{ or } 3; \end{cases} \quad \prod_{i=1}^m L_3(a_i) = \begin{cases} 1 & \text{if } \forall i \ a_i = 3; \\ 0 & \text{if } \exists i \ a_i = 0, 1 \text{ or } 2; \end{cases}$$

$$\prod_{i,p,k,s=1}^m L_0(a_i).L_1(a_p).L_2(a_k).L_3(a_s) = \begin{cases} 1 & \text{if } \forall i, p, k, s \ a_i = 0, a_p = 1, a_k = 2, a_s = 3; \\ 0 & \text{if } \exists i, p, k, s \ a_i = 1, 2 \text{ or } 3, a_p = 0, 2 \text{ or } 3; \\ & a_k = 0, 1 \text{ or } 2, a_s = 0, 1 \text{ or } 2; \end{cases}$$

where  $i + p + k + s = m$ .

Hence, the minterms for which  $f = 1$  are

1.  $\prod_{i=1}^m L_0(a_i = 0)$ , 2.  $\prod_{i=1}^m L_1(a_i = 1)$ , 3.  $\prod_{i=1}^m L_2(a_i = 2)$ ,
4.  $\prod_{i=1}^m L_3(a_i = 3)$ , 5.  $\prod_{i,p,k,s=1}^m L_0(a_i = 0).L_1(a_p = 1).L_2(a_k = 2).L_3(a_s = 3)$ .

Similarly from Table 2, the minterms for which  $f = 2$  are

1.  $\prod_{i=1}^m J_0(a_i = 0)$ , 2.  $\prod_{i=1}^m J_1(a_i = 1)$ , 3.  $\prod_{i=1}^m J_2(a_i = 2)$ ,
4.  $\prod_{i=1}^m J_3(a_i = 3)$ , 5.  $\prod_{i,p,k,s=1}^m J_0(a_i = 0).J_1(a_p = 1).J_2(a_k = 2).J_3(a_s = 3)$ .

The minterms for which  $f = 3$  are

1.  $\prod_{i=1}^m P_0(a_i = 0)$ , 2.  $\prod_{i=1}^m P_1(a_i = 1)$ , 3.  $\prod_{i=1}^m P_2(a_i = 2)$ ,
4.  $\prod_{i=1}^m P_3(a_i = 3)$ , 5.  $\prod_{i,p,k,s=1}^m P_0(a_i = 0).P_1(a_p = 1).P_2(a_k = 2).P_3(a_s = 3)$ .

## 4.2 Simplification Rules

Next, we define six simplification rules derived from Table 2

1.  $L_i(a).0 = 0$ ,  $J_i(a).0 = 0$  and  $P_i(a).0 = 0$
2.  $L_i(a).1 = L_i(a)$ ,  $J_i(a).2 = J_i(a)$  and  $P_i(a).3 = P_i(a)$
3.  $L_i(a) + 0 = L_i(a)$ ,  $J_i(a) + 0 = J_i(a)$  and  $P_i(a) + 0 = P_i(a)$
4.  $L_i(a) + 1 = 1$ ,  $J_i(a) + 2 = 2$  and  $P_i(a) + 3 = 3$
5.  $L_i(a).L'_i(a) = 0$ ,  $J_i(a).J'_i(a) = 0$  and  $P_i(a).P'_i(a) = 0$
6.  $L_i(a) + L'_i(a) = 1$ ,  $J_i(a) + J'_i(a) = 2$  and  $P_i(a) + P'_i(a) = 3$

**Simplification Rules for reducing ancilla qudits** For gate level realization of  $L_i$ ,  $J_i$ , and  $P_i$  we need an ancilla qudit for each of them. Further, to synthesize an  $m$ -variable quaternary function with  $n$  minterms specified in our proposed methodology, we have maximum of  $n * m$  ancilla qudits. However, we can reduce the number of ancilla qudits by the following three simplification rules based on the new quaternary  $C^2CS$  gate and Table 2:

$$7. L_i(a)L_j(b) + L_j(a)L_i(b) = C^2CS(a_{ij}, b_{ij}, 0), J_i(a)J_j(b) + J_j(a)J_i(b) = C^2CS(a_{ij}, b_{ij}, 1) \text{ and } P_i(a)P_j(b) + P_j(a)P_i(b) = C^2CS(a_{ij}, b_{ij}, 2) \text{ Where } i, j = \{1, 2, 3\}$$

$$8. L_i(a).L_i(a) = L_i(a), J_i(a).J_i(a) = J_i(a) \text{ and } P_i(a).P_i(a) = P_i(a)$$

$$9. L_i(a_1)L_i(a_2)..L_i(a_n) = L_i(a_1, a_2, \dots, a_n), J_i(a_1)J_i(a_2)..J_i(a_n) = J_i(a_1, a_2, \dots, a_n), \text{ and } P_i(a_1)P_i(a_2)..P_i(a_n) = P_i(a_1, a_2, \dots, a_n), i = \{0, 1, 2, 3\}.$$

## 5 Synthesis of Quaternary Functions

### 5.1 2-qudit Quaternary Arbitrary Function

The truth table for the 2-qudit arbitrary function  $f(a, b)$  is given in Table 4.

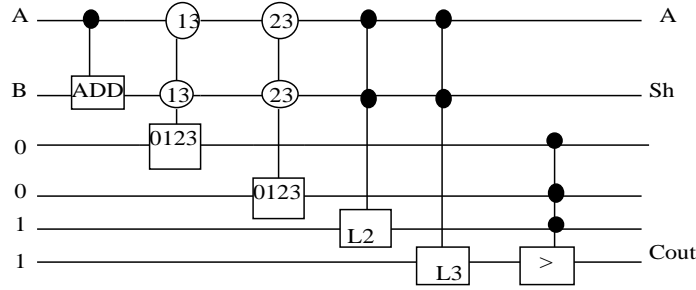
**Table 4.** Truth table of 2-qudit  $f(a, b)$

a, b	00	01	02	03	10	11	12	13	20	21	22	23	30	31	32	33
$f(a, b)$	0	3	1	2	3	3	2	0	1	2	1	3	2	1	3	2

We re-write the function  $f(a, b)$  using our proposed methodology as  
 $f(a, b) = L_0(a)L_2(b) + L_2(a)L_0(b) + L_2(a)L_2(b) + L_3(a)L_1(b) + J_0(a)J_3(b) + J_1(a)J_2(b) + J_2(a)J_1(b) + J_3(a)J_0(b) + J_3(a)J_3(b)P_0(a)P_1(b) + P_1(a)P_0(b) + P_1(a)P_1(b) + P_2(a)P_3(b) + P_3(a)P_2(b)$

By using simplification rules 7 and 9, we get

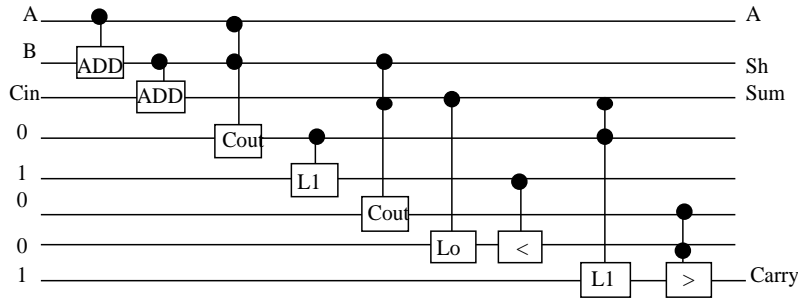
$$f(a, b) = C^2CS(a_{02}, b_{02}, 0) + L_2(a, b) + L_3(a)L_1(b) + C^2CS(a_{03}, b_{03}, 1) + C^2CS(a_{12}, b_{12}, 1) + J_3(a, b) + C^2CS(a_{10}, b_{10}, 2) + C^2CS(a_{23}, b_{23}, 0) + P_1(a, b)$$



**Fig. 8.** Quaternary 2-qudit Half Adder by our synthesis method

### 5.2 Quaternary Adder

We synthesize the 2-qudit half and full adder circuits using our proposed methodology and these circuits are simplified with the use of Modulo4 Addition gate. But the details are not provided due to limitation of space. The gate level implementation of 2-qudit half and full adder are shown in Figure 8 and 9 respectively.



**Fig. 9.** Quaternary 2-qudit Full Adder by our synthesis method

### 5.3 Comparison of Results

The quantum cost of the half and the full adder circuits, as shown in Figures 10 and 11, and of the benchmark circuits such as *sum2*, *rd53*, *rd73*, *xor5* are



evaluated in terms of the number of M-S gates used. The number of M-S gates required to realize a 2-qudit Feynman gate, a 3-qudit Toffoli, *MAX* and *MIN* gates are 5, 17, 6, 6 respectively [7,13]. To realize the new GQG, *C<sup>2</sup>CS*, ADD gates we need 8 M-S gates for each of them. The M-S gate count cost comparison of our circuits with that in [14] are given in Table 6. While the second column of the table indicates the maximum number of ancilla qudits required to synthesize the above mentioned circuits, the third column shows the number of ancilla qudits required after using our simplification rules in Section 4.2. The columns 4, 5 and 6 establish that although our design has a small increase in cost for the circuits *rd53*, *rd73*, *xor5*, the results for the 2-qudit quaternary half and full adder shows that there is more than 50% reduction in the M-S gate count cost compared to [14].

**Table 5.** Comparison of Quantum cost by our method vs. [14]

Circuit	maximum ancilla qudits	Reduced ancilla qudits	# Levels		Total Cost	
			Ours	[14]	Ours	[14]
Half Adder	36	6	6	23	46	114
Full Adder	120	17	17	40	128	304
Sum2	24	0	4	-	8	-
mul2	16	5	5	-	40	-
ham3	135	95	25	-	135	-
rd53	275	245	15	-	120	-
rd73	475	435	35	-	280	-
xor5	150	120	7	-	56	-

## 6 Conclusion

In this paper, we have proposed a methodology for logic synthesis of quaternary quantum circuits. We have defined a minterm based approach of expressing a quaternary logic function using  $L_i$ ,  $J_i$  and  $P_i$  operations. We have also stated the simplification rules for the method. Quaternary half adder, full adder and some benchmark circuits synthesized by our method, use fewer ternary quantum gates and hence reduce quantum realization cost compared to earlier method in [14]. While the number of levels is fewer in our synthesis, the number of ancilla bits is higher. A synthesis methodology for reduction of the number of ancilla qudits is being investigated.

## References

1. M. A. Nielsen and I. L. Chuang, *Quantum Computation and Quantum Information*, Cambridge University Press, 2002.
2. A. Ekert and A. Zeilinger, *The physics of quantum information*, Springer Verlag, Berlin, 2002, pp. 1-14.
3. A. Muthukrishnan and C. R. Stroud Jr., *Multi-Valued Logic Gates for Quantum Computation*, Phys. Rev. A62, 2000, pp. 0523091-8.
4. P. Picton, *A Universal Architecture for Multiple-Valued Reversible Logic*, Multiple-Valued Logic - An International Journal, Vol. 5, 2000, pp. 27-37

5. J. L. Brylinski and R. Brylinski, *Universal Quantum Gates*, (to appear in Mathematics of Quantum Computation, CRC Press, 2002) LANL e-print quant-ph/010862.
6. M. Perkowski, A. Al-Rabadi, P. Kerntopf, A. Mishchenko, and M. Chrzanoska-Jeske, *Three-Dimensional Realization of Multivalued Functions Using Reversible Logic*, Booklet of 10th Int. Workshop on Post-Binary Ultra-Large-Scale Integration Systems (ULSI), Warsaw, Poland, May 2001, pp.47- 53
7. M.M.M Khan, A. K. Biswas, S. Chowdhury, M.Tanzid, K.M.Mohsin, M. Hasan, A. I. Khan , *Quantum realization of some quaternary circuits*, TENCON 2008 - 2008 IEEE Region 10 Conference , vol., no., pp.1-5, 19-21 Nov. 2008
8. M. H. Khan, *Quantum Realization of Quaternary Feynman and Toffoli Gates* Electrical and Computer Engineering, 2006. ICECE '06. International Conference on , vol., no., pp.157-160, 19-21 Dec. 2006
9. M. H. Khan, *Synthesis of incompletely specified multi-output quaternary function using quaternary quantum gates*, Computer and information technology, 2007. iccit 2007. 10th international conference on , vol., no., pp.1-6, 27-29 Dec. 2007
10. M.H.A. Khan, N.K. Siddika, M.A. Perkowski, *Minimization of Quaternary Galois Field Sum of Products Expression for Multi-Output Quaternary Logic Function Using Quaternary Galois Field Decision Diagram*, Multiple Valued Logic, 2008. IS-MVL 2008. 38th International Symposium on , vol., no., pp.125-130, 22-24 May 2008
11. S.B.Mandal, A. Chakrabarti, and S. Sur-Kolay, *Synthesis Technique for Ternary Quantum Logic*, 41 th International Symposium on Multiple-Valued Logic, Tuusula, 2011, pp. 218-223.
12. R. L. Herrmann, *Selection and implementation of a ternary switching algebra*, Spring Joint Computer Conference, Atlantic City, 1968, pp. 283-290 .
13. N. Giesecke, D. H. Kim, S. Hossain and M. Perkowski, *Search for Universal Ternary Quantum Gate Sets with Exact Minimum Costs*, Proceedings of RM Symposium, Oslo, May 16, 2007.
14. M. H. A. Khan, *A recursive method for synthesizing quantum/reversible quaternary parallel adder/subtractor with look-ahead carry* Journal of Systems Architecture 54 (2008) 11131121 .