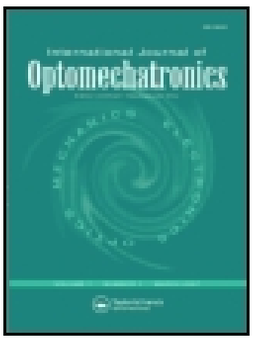

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ALL-OPTICAL INCREMENTER/DECREMENTER WITH THE HELP OF SEMICONDUCTOR OPTICAL AMPLIFIER-ASSISTED SAGNAC SWITCH

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In this article, an all-optical adder based incrementer\decrementer circuit is proposed and described with the help of Semiconductor Optical Amplifier (SOA)-assisted Sagnac switch. The proposed design is more efficient in terms of speed and hardware complexity. The article describes the incrementer\decrementers using a set of optical half adder and full adder. The principle and possibilities of all-optical incrementer\decrementers is explained. A theoretical model is presented and verified through numerical simulation. The new method promises both higher processing speed and accuracy. The model can be extended for studying more complex all-optical circuit of enhanced functionality in which incrementer\decrementers is the basic building block.

Keywords: optical full adder, optical half adder, optical incrementer/decrementers, semiconductor optical amplifier, Terahertz optical asymmetric demultiplexer

1. INTRODUCTION

The incrementer/decrementer (INC/DEC) is a digital module which can count up or count down by one step in one clock cycle. It is a common building block in digital system and finds many applications such as the program counter and the frequency divider. INC/DEC is also used in many digital systems like address generation units which are used in microcontrollers and microprocessors. The new method promises both higher processing speed and accuracy. The binary INC/DEC implements the function of $Y = Z \pm 1$ where Z is the input integer number. The current implementations of INC/DECs are mainly adder-based. For the adder-based INC/DECs, the operating speed limitation comes from the inherent carry propagation of adders. All-optical INC/DECs have many potential

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NOMENCLATURE

SOA	semiconductor optical amplifier	C.R.	contrast ratio
INC/DEC	incrementer/decrementer	*BER*	bit error rate
TOAD	terahertz optical asymmetric demultiplexer	CPLS	constant pulse light source
OTDM	optical time division multiplexing	E_{cw}	clockwise incoming pulse
NLE	non linear element	E_{ccw}	counter clockwise incoming pulse
CP	control pulse	G_{ss}	unsaturated single-pass amplifier gain
CW	clockwise		
CCW	counter clockwise	τ_e	gain recovery time
FWHM	full width at half maximum	E_{sat}	saturation energy of the SOA
PC	polarization controllers	T	eccentricity of the loop of TOAD
PF	polarization filter	E_{cp}	control pulse energy
H.A.	half adder	T_c	bit period
F.A.	full adder	σ	full width at half maximum of control pulse
B.C.	beam combiner		

applications in optical communication and computing system. Various architectures, algorithms, logical, and arithmetic operations have been proposed in the field of optical/optoelectronic computing and parallel signal processing in last few decades (Agrwal 2001; Guoqiang et al. 1999; Sokoloff et al. 1993; Zoiros et al. 2004). Among the proposed schemes, the terahertz optical asymmetric demultiplexer (TOAD)/semiconductor optical amplifier (SOA)-assisted Sagnac gate effectively combines fast switching time and a reasonable noise figure, with the ease of integration and overall practicality that enables it to compete favorably with other similar optical time division multiplexing (OTDM) devices. TOAD is characterized by the attractive features of fast switching time, high repetition rate, low power consumption, low latency, noise and jitter tolerance, compactness, thermal stability, and high nonlinear properties, which enable their efficient exploitation in a real ultra-high speed optical communications environment (Stubkjaer 2000). TOAD have the potential of being integrated, which in turn means that they can be repeatedly and reliably manufactured and massively produced so that they can be of commercial value and favorably compete with other buffering solutions (Zoiros et al. 2006; Glesk et al. 2001). In our previously published article, we proposed TOAD-based tree architecture for all-optical logic and arithmetic operations (Roy and Gayen 2007), all-optical arithmetic unit (Gayen and Roy 2008) and all-optical adder/subtractor unit (Gayen et al. 2009). In this article we propose and describe the TOAD-based switch to design an integrated circuit which can perform binary incrementer/decrementer in all-optical domain. The circuit has been thoroughly investigated through numerical simulation. Variation of contrast ratio has been studies with different values of control pulse energy, eccentricity of the loop and gain recovery time. The variation of bit error rate with different values of control pulse energy has also been investigated.

The article is organized as follows. In Section 2, principle and operation of TOAD based optical switch is discussed. All-optical half adder and full adder is reported in Section 3. Designing of all-optical binary incrementer/decrementer is described in Section 4. Numerical simulation result (by Matlab6.5) and discussion is reported in Section 5. The conclusion is given in Section 6.

2. OPERATIONAL PRINCIPLE OF TOAD-BASED OPTICAL SWITCH

An interferometric switch consists of two 3-dB couplers. The first coupler splits the input into two distinct arms. The arms of the interferometer are of the same lengths. The input beam is allowed to travel in these two distinct paths. Another coupler is placed to combine the beams and finally split the signal again. A change in the index adds a phase shift between the two arms of the interferometer. Therefore, a phase difference between two optical beams is created. This produces interference, which may be constructive or destructive. Hence the power on alternate outputs becomes maximum or minimum. By proper selection of output beam, the device acts as an optical switch. Optical switch using a nonlinear interferometer makes it possible for one optical signal to control and switch another optical signal through the nonlinear interaction in a material. The incoming signal to be switched is split between the arms of the interferometer. The interferometer is balanced so that, in the absence of a control signal, the incoming signal emerges from one output port. The presence of a strong control pulse changes the refractive index of the medium. Light is passed through the medium. In this case the medium is optical fiber and semiconductor optical amplifier (InGaAsP) which is placed asymmetrically in the fiber loop. Here the function of the SOA is not to amplify but to produce a large phase shift in the signal. The refractive index of some kind of nonlinear materials can be expressed as

$$n = n_0 + n_2 I$$

where n_0 is a constant term, n_2 is coefficient of nonlinear correction term and I is the intensity of input light beam. Hence,

$$\Delta n = n - n_0 = n_2 I$$

where Δn is the change in the refractive index of the medium. A change in the index adds a phase shift between the two arms of the interferometer, so that the incoming signal is switched over to another output port.

In recent years, the TOAD-based gate has taken an important role in the field of optical communication and information processing (Chattopadhyay and Roy 2008; Chattopadhyay et al. 2009a,b; Sokoloff et al. 1994; Zoiros et al. 2007; Houbavlis and Zoiros 2003a,b; Zoiros et al. 2005a,b; Menon et al. 2003). Sokoloff et al. (1993) demonstrated a new device, the terahertz optical asymmetric demultiplexer (TOAD) capable of demultiplexing data at 50 Gbits/s. TOAD exploits the strong, slow optical nonlinearities present in semiconductor and permits control and signal pulses to be distinguished by polarization or wavelength, and it requires less than 1 pJ switching energy. The same group has also demonstrated that by reducing the SOA length to 100 μm and increasing its dc bias current, its propagation delay can be reduced to 1 ps without impacting its performance as an NLE (non linear element), then TOAD can perform Tb/s demultiplexing (Sokoloff et al. 1993). The TOAD consists of a loop mirror with an additional, intra-loop 2×2 (ideally 50:50) coupler (Sokoloff et al. 1993). The loop contains a control pulse (CP) of different light than that of the incoming pulse and a semiconductor optical amplifier (SOA) that is offset from the loop's midpoint by a distance Δx as shown

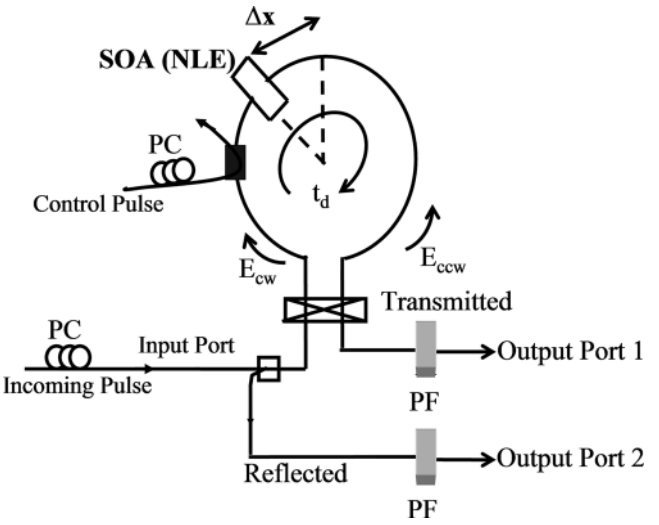

Figure 1. TOAD-based optical switch. PC: Polarization Controller, PF: Polarization Filter, Ecw: clockwise incoming pulse, E_{ccw}: counter clockwise incoming pulse, SOA: Semiconductor Optical Amplifier, NLE: Non Linear Element, ■: Polarization selective Coupler, ⟳: Optical Circulator, ⊠: 3-dB Coupler, t_d: Pulse round trip time within the loop.

in Figure 1. In the absence of a control signal, incoming signals enter the fiber loop, pass through the SOA at different times as they counter-propagate around the loop, and recombine interferometrically at the coupler. Since both signals see the same medium as they propagate around the loop, the data is reflected back toward the source. When a control signal is injected into the loop, it saturates the SOA and changes its index of refraction. As a result, a differential phase shift can be achieved between the two counter-propagation signals to switch the incoming signal which is transmitted to output port 1.

Menon and his research group are working in this field to reduce the size of TOAD and to integrate it (Houbavlis and Zoiros 2003b; Menon et al. 2003). The device fabrication consists of three ion-etching steps to define the shallow-ridge active waveguide in the SOA regions, the taper couplers, and the passive waveguide. The wafer is planarized using silicon nitride. Electron beam evaporation was used to deposit Ti-Ni-Au p-contacts extending over the entire active ridge including the tapers. The *p*-contacts are annealed at 415°C for 30 s. The wafer is thinned to 130 μm and annealed at 360°C for 90 s. The size of the device is 1.5 mm × 3.5 mm and is primarily determined by the bend radius of the dilute waveguide. In almost all TOAD discussed by many authors, the transmitting mode of the device (output port) is used to take the output signal. But the signal that exits from the input port (reflecting mode) remains unused. In our earlier article we tried to utilize the output from both the transmitting and reflecting mode of the device (Roy and Gayen 2007; Gayen and Roy 2008; Gayen et al. 2009; Chattopadhyay and Roy 2008; Chattopadhyay et al. 2009a,b) to perform logical arithmetic operations. In this present communication we have tried to use the output from both the transmitting and reflecting mode of the device. The output power at port-1 and port-2 can be

expressed as (Eiselt et al. 1995; Huang et al. 2006),

$$P_{out}(t) = \frac{P_{in}(t)}{4} \cdot \left\{ G_{cw}(t) + G_{ccw}(t) \mp 2\sqrt{G_{cw}(t) \cdot G_{ccw}(t)} \cdot \cos(\Delta\varphi) \right\} \tag{1}$$

where $G_{cw}(t)$, $G_{ccw}(t)$ are the power gain exhibited by the clockwise (CW) and counter clockwise (CCW) pulses, respectively. The time-dependent phase difference between CW and CCW pulses (Eiselt et al. 1995) is

$$\Delta\varphi = -\frac{\alpha}{2} \cdot \ln(G_{cw}(t)/G_{ccw}(t)) \tag{2}$$

with α being the line-width enhancement factor. In the absence of a control signal, data signals (incoming signal) enter the fiber loop, pass through the SOA at different times as they counter-propagate around the loop, and experience the same unsaturated small amplifier gain G_{ss}, and recombine at the input coupler i.e., $G_{ccw} = G_{cw}$. Then, $\Delta\varphi = 0$ and expression for $P_{out,1}(t) = 0$ and $P_{out,2}(t) = P_{in}(t) \cdot G_{ss}$. It shows that data is reflected back toward the source. When a control pulse is injected into the loop, it saturates the SOA and changes its index of refraction by the formula (Agrwal 2001; Eiselt et al. 1995)

$$G(t) = \frac{1}{1 - \left(1 - \frac{1}{G_{ss}}\right) \exp\left(\frac{E_{cp}(t)}{E_{sat}}\right)}; \quad t \le t_s \tag{3}$$

where E_{sat} is the saturation energy of the SOA and $E_{cp}(t) = \int_{\infty}^{t} P_{cp}(t')dt'$. Here we consider Gaussian pulse $P_{cp}(t) = \frac{E_{cp}}{\sigma\sqrt{\pi}} \exp\left(-\frac{t^2}{\sigma^2}\right)$ as control signal. E_{cp} is the control pulse energy. σ is the full width at half maximum (FWHM). As a while the gain recover due to injection of carriers and can be obtained from the gain recovery formula (Agrwal 2001; Eiselt et al. 1995)

$$G(t) = G_{ss}\left(\frac{G(t_s)}{G_{ss}}\right)^{\exp\left(-\frac{(t-t_s)}{\tau_e}\right)}; \quad t \ge t_s \tag{4}$$

where τ_e is the gain recovery time and t_s is the saturation time of SOA. As a result, the two counter-propagation data signals will experience a differential gain

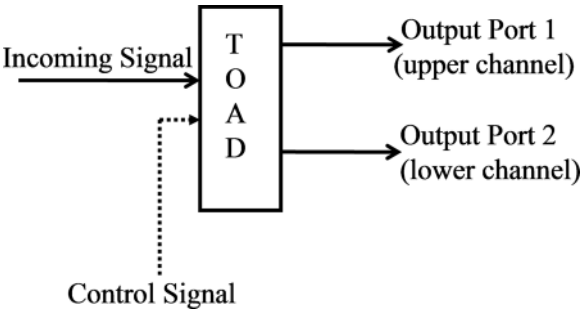

Figure 2. Schematic diagram of TOAD-based optical switch.

Table 1. Truth table of Figure 1

Incoming Signal	Control Signal	Output Port-1	Output Port-2
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	0

saturation profile i.e., $G_{ccw} \neq G_{cw}$. Therefore they recombine at the input coupler, and then $\Delta\varphi \approx \pi$ the data will exit from the output port-1 i.e., $P_{out,1}(t) \neq 0$ and $P_{out,2}(t) \approx 0$, the corresponding values can be obtained from Eq. (1). The control pulse and incoming pulse can be discriminated by appropriately adjusting their polarization states by means of polarization controllers (PC) so that they are orthogonal to each other. The output of any switch can be used as an incoming/control pulse for the other provided they are passed through variable optical attenuator and polarization controller. A polarization filter (PF) may be used at the output of TOAD-based switch to reject the control and pass the incoming pulse. The block diagram is shown in the Figure 2. The truth table of Figure 1 is given in Table 1. Now it is clear that in the absence of the control signal, the incoming pulse exits through the reflected port of TOAD and reaches output port-2. In this case no light is present in output port-1. But in the presence of the control signal the incoming signal exits through transmitted port of TOAD and reaches output port-1. In this case no light is present in output port-2. In the absence of the incoming signal, port-1 and port-2 receive no light as the filter blocks the control signal. An additional requirement for a pulse to be fully transmitted is that its width σ must be as short as possible and ideally less than the switching window, so that when the CCW pulse is inserted into the SOA, the CW pulse has already passed through and the SOA gain has started recovering after saturation by the control pulse. Moreover, the eccentricity (T) i.e., asymmetry of SOA in the loop must be less than the gain recovery time τ_e, so that the CCW enters the SOA before carrier recombination is completed to experience a different gain and acquire the required phase shift. In order to achieve optimum operation the eccentricity must be less than half the clock bit period T_c. The simultaneous satisfaction of all these condition is expressed by

$$\sigma < T < 0.5T_c < \tau_e < 1.5T_c \quad \text{and} \quad \Delta x = \frac{T}{2} \tag{5}$$

3. ALL-OPTICAL HALF ADDER AND FULL ADDER

We know that a half-adder has two inputs (A and B) and produces two outputs representing "sum (S)" and "carry (C)". In our earlier article (Roy and Gayen 2007), we reported three TOAD-based switches for designing an all-optical half-adder (H.A.) (Figure 3). "Sum" takes the expression $\overline{A}B + A\overline{B}$ and "carry" takes the expression AB. Hence by combining the output of T-2 and T-3 with a beam combiner (BC) we can get the "sum" bit. At the same time T-4 gives the "carry" bit. The full-adder circuit adds

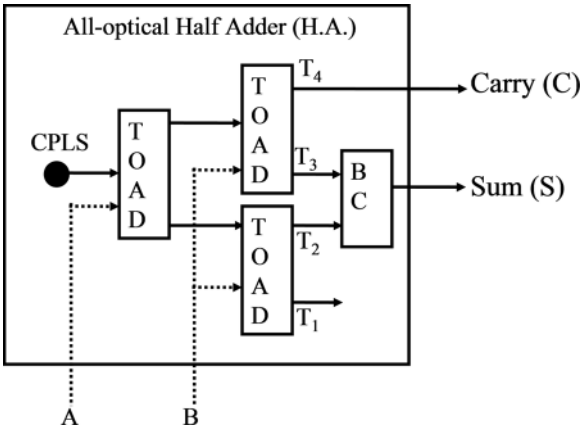

Figure 3. All-optical half adder. CPLS: Constant pulse light source, B.C.: Beam combiner.

three one-bit binary numbers (A, B, C_{in}) and gives the outputs in two one-bit binary numbers, a "sum (S)" and a "carry (C_{out})." The operational principle of one bit optical full-adder has been explained in Roy and Gayen (2007) and Gayen and Roy (2008). The schematic diagram is shown in Figure 4.

4. PRINCIPLE AND DESIGN OF ALL-OPTICAL INCREMENTER/DECREMENTER

All-optical 4-bit binary INC/DEC with the help of optical half adder and full adder is shown in Figure 5. This optical circuit can perform INC/DEC with 4-bit

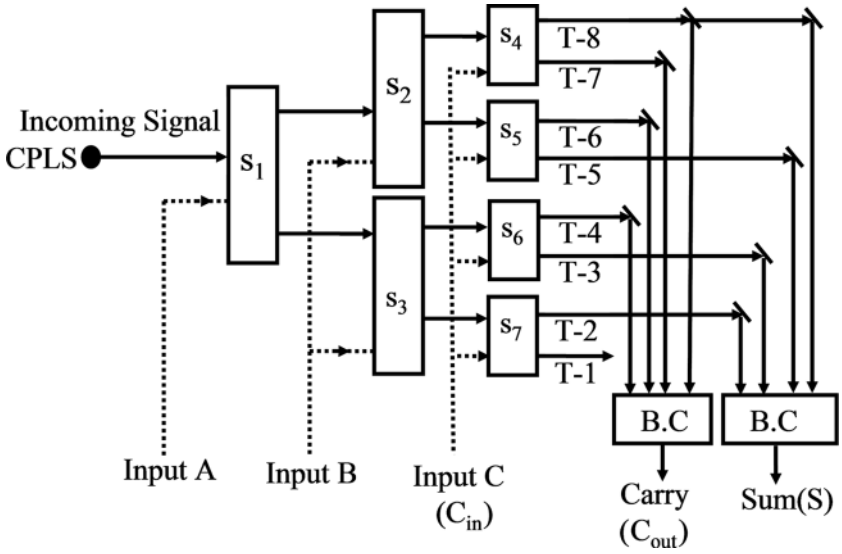

Figure 4. Optical circuit for 1-bit all-optical full-adder. B.C.: Beam Splitter.

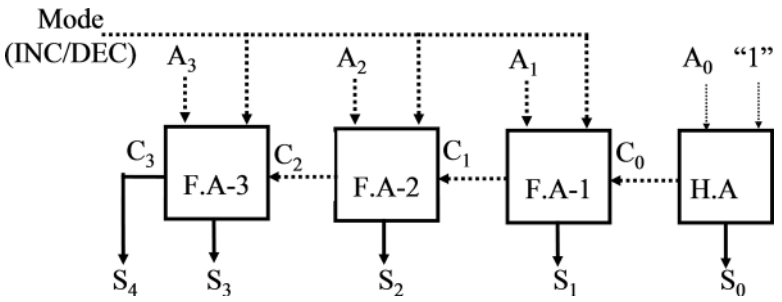

Figure 5. All-optical binary incrementer/decrementer. F.A: Full adder, H.A: Half adder.

input number A ($A_3A_2A_1A_0$). It gives the output S ($S_4S_3S_2S_1S_0$) depending on the value of mode (INC/DEC). Let us consider an example where $A = 1001(A_3A_2A_1A_0)$. The operational principles of two cases are described in details.

Case 1. mode (INC/DEC) = 0

Here, the half adder H.A. receives the value of two inputs as 1 (as $A_0 = 1$) and 1 (as one input always in one (high) state). According to the operational principle of half adder, it generates the output as zero i.e., $S_0 = 0$ and carry out as one i.e., $C_0 = 1$. One input of the full adders FA-1, FA-2, and FA-3 receive the value 0 as the mode (INC/DEC) = 0. So the full adder FA-1 receives the value of three inputs as 0 (as $A_1 = 0$), 0 (as INC/DEC = 0), and 1 (as $C_0 = 1$). According to the operational principle of full adder, the output S_1 takes the value one i.e., $S_1 = 1$ and carry out receives the value zero i.e., $C_1 = 0$. The full adder FA-2 receives the value of three inputs as 0 (as $A_2 = 0$), 0 (as INC/DEC = 0), and 0 (as $C_1 = 0$). So in this case it produces the output sum as zero i.e., $S_2 = 0$ and carry out receives the value zero i.e., $C_2 = 0$. Finally the FA-3 receives the value of three inputs as 1 (as $A_3 = 1$), 0 (as INC/DEC = 0), and 0 (as $C_2 = 0$). Hence $S_3 = 1$ and $C_3 = 0$. Here the output S_4 takes the value 0 as $C_3 = 0$. The final output (S) is 01010 ($S_4S_3S_2S_1S_0$) that verifies the incrementer operation.

Case 2. mode (INC/DEC) = 1

Here, the half adder H.A. receives the value of two inputs as 1 (as $A_0 = 1$) and 1 (as one input always in one (high) state). It generates the output as zero i.e., $S_0 = 0$ and carry out as one i.e., $C_0 = 1$. One input of the full adders FA-1, FA-2, and FA-3 receive the value 1 as the mode (INC/DEC) = 1. So the full adder FA-1 receives the value of three inputs as 0 (as $A_1 = 0$), 1(as INC/DEC = 1), and 1 (as $C_0 = 1$). Here, the output S_1 takes the value zero i.e., $S_1 = 0$ and carry out receives the value one i.e., C_1=1. The full adder FA-2 receives the value of three inputs as 0 (as $A_2 = 0$), 1 (as INC/DEC = 1), and 1 (as $C_1 = 1$). So in this case it produces the output sum as zero i.e., $S_2 = 0$ and carry out receives the value one i.e., $C_2 = 1$. Finally the FA-3 receives the value of three inputs as 1 (as $A_3 = 1$), 1 (as INC/DEC = 1), and 1 (as $C_2 = 1$), so $S_3 = 1$ and $C_3 = 1$ i.e., $S_4 = 1$. So it generates the output S as 11000 ($S_4S_3S_2S_1S_0$). As A is a 4-bit number the final result will also in 4-bit form and hence the final carry (S_4) is to be discarded. Here, the final result is 1000 ($S_3S_2S_1S_0$) that verifies decrementer operation.

5. RESULT AND DISCUSSION

The different parameters used in simulation have been taken from the literature that reports experimental results (Zoiros et al. 2007; Houbavlis and Zoiros 2003a,b; Eiselt et al. 1995). For this simulation the values of the parameters as unsaturated single-pass amplifier gain $(G_{ss}) = 20\,\text{dB}$, Line-width enhancement factor of SOA $(\alpha) = 6$, $\tau_e = 50\,\text{ps}$, full width at half maximum of control pulse $(T_{FWHM}) = 3.33\,\text{ps}$, eccentricity of the loop $(T) = 30\,\text{ps}$ and a control energy of 70 fJ so that the operational conditions are satisfied. Results of simulations at different stages are given in Figures 6 to 9. In Figure 4, let us consider switch s_1 as stage 1, the switches s_2 and s_3 as stage 2 and the switches s_4 to s_7 as stage 3. Figure 6 gives the variation of contrast ratio (C.R.) with different values of control pulse energy (E_{cp}) at different stages and output of the Figure 4 when, eccentricity of the loop

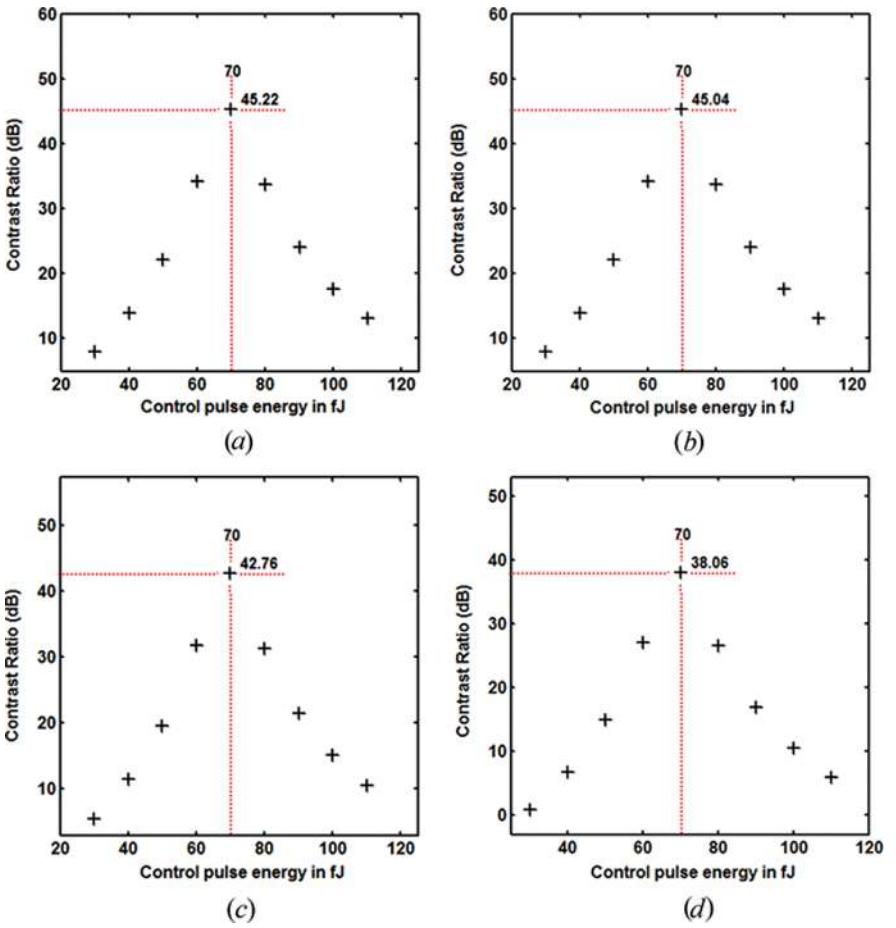

Figure 6. The variation of contrast ratio (C.R.) with control pulse energy (E_{cp}) at different stages. 6(a): in stage 1 (i.e., the switch s_1 in Figure 4), 6(b): in stage 2 (i.e., the switches s_2 and s_3 in Figure 4), 6(c): in stage 3 (i.e., the switches s_4 to s_7 in Figure 4), 5(d): in the output of Figure 4.

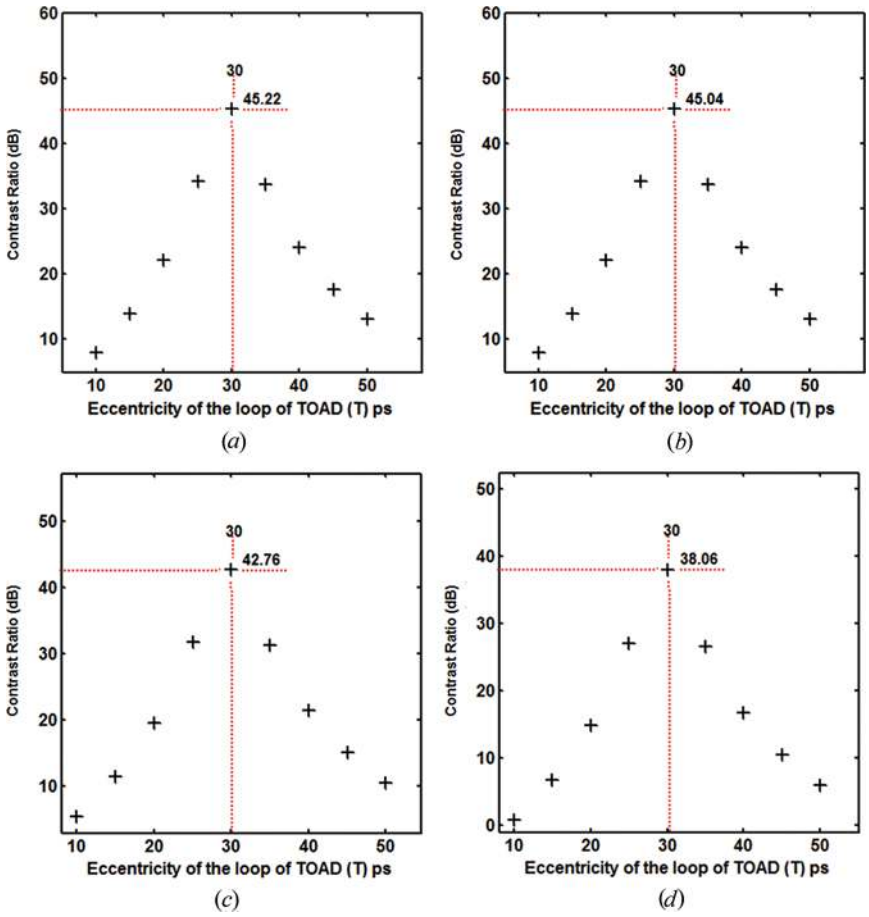

Figure 7. The variation of contrast ratio (*C.R.*) with Eccentricity of the loop (T) at different stages. 7(a): in stage 1 (i.e., the switch s_1 in Figure 4), 7(b): in stage 2 (i.e., the switches s_2 and s_3 in Figure 4), 7(c): in stage 3 (i.e., the switches s_4 to s_7 in Figure 4), 7(d): in the output of Figure 4.

(T) is kept constant. The maximum value of C.R. in stage 1 is about 45.22, stage 2 is about 45.04, stage 3 is about 42.76, and finally it is about 38.06. This shows that the C.R. decreases with the increase of cascades stages. Figure 7 gives the variation of contrast ratio (C.R.) with eccentricity of the loop (T), when E_{cp} is kept fixed. This also shows that the C.R. decreases with the increase of cascades stages. Figure 8 gives the variation of contrast ratio (C.R.) with gain recovery time (τ_e), when other parameters are kept fixed. This shows that the C.R. decreases with the increase of cascades stages. Figure 9 gives the variation of bit error rate with different values of control energy at stage 1 and stage 2 and its minimum value is about 10^{-15}. The developed model (Figure 5) can handle arbitrary data patterns A ($A_3A_2A_1A_0$). For example we have taken two set of inputs where $A = 1001$ and $A = 1111$, the corresponding output waveform are shown in Figure 10. Figure 10(a) shows the output waveform when $A = 1001$, 1111, and mode (INC/DEC) = 04. Figure 10(b)

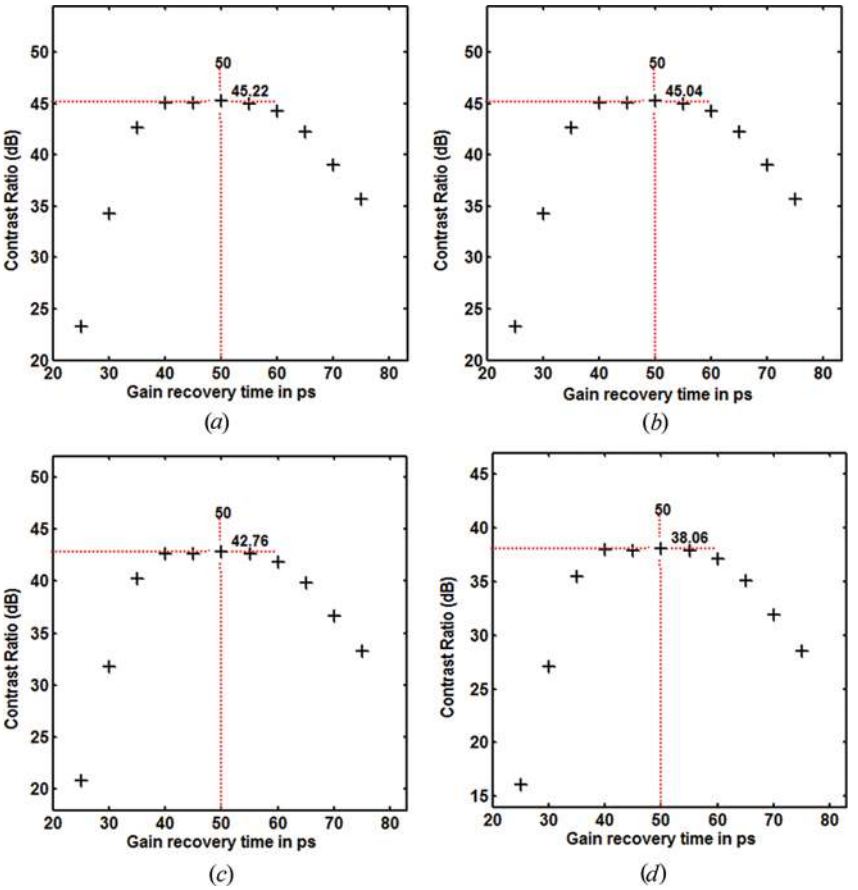

Figure 8. The variation of contrast ratio (*C.R.*) with gain recovery time (τ_e) at different stages. 8(a): in stage 1 (i.e., the switch s_1 in Figure 4), 8(b): in stage 2 (i.e., the switches s_2 and s_3 in Figure 4), 8(c): in stage 3 (i.e., the switches s_4 to s_7 in Figure 4), 8(d): in the output of Figure 4).

shows the output waveform when $A = 1001$, 1111, and mode (INC/DEC) = 1. In order to assess the performance of the optical circuit at 20 Gb/s, the quality of optical circuit (Figure 5) output are defined and calculated. We select the output contrast ratio (C.R.) as the optimization criteria, which indicate the opening of the eye diagram and is defined as

$$C.R.(dB) = 10\log\left(\frac{P^1_{Min}}{P^0_{Max}}\right) \tag{6}$$

where P^1_{Min} and P^0_{Max} is the minimum and maximum value of the peak power of '1' and '0', respectively. From equation (6) we can calculate the output $C.R.(dB)$ for INC/DEC and is found 38.06 dB. Figure 11 gives the variation of *C.R.* with control pulse energy (E_{cp}) when, eccentricity of the loop (T) is kept constant. It shows that maximum *C.R.* is obtained at 70 fJ control pulse energy. Here we see that

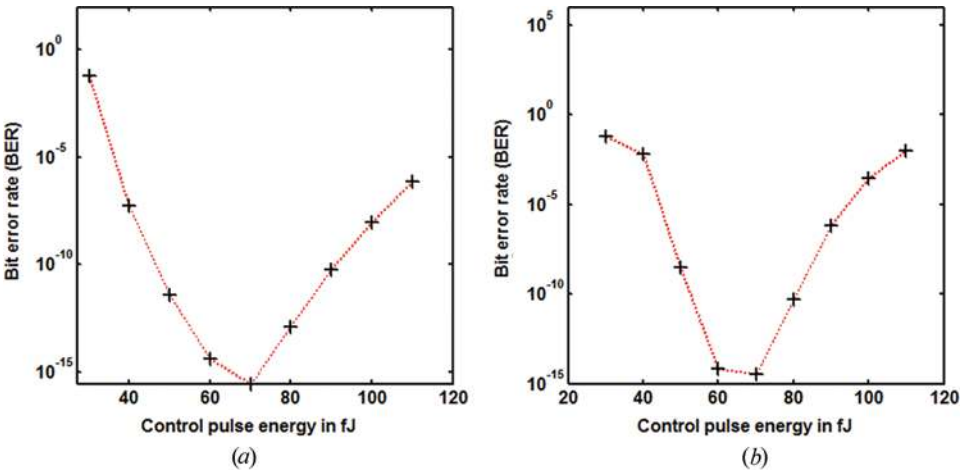

Figure 9. The variation of bit error rate (BER.) with control pulse energy (E_{cp}) at different stages. 9(a): in stage 1 (i.e., the switch s_1 in Figure 4), 9(b): in stage 2 (i.e., the switches s_2 and s_3 in Figure 4).

C.R. increases rapidly first and then decrease after $E_{cp} \sim 70$ fJ. Figure 12 shows the variation of *C.R.* with T, when E_{cp} is fixed and it confirms that *C.R.* is high when eccentricity of the loop (T) is 30 ps. Figure 13 shows the variation of contrast ratio (*C.R.*) with gain recovery time (τ_e), when other parameters are kept fixed. It shows that maximum *C.R.* is obtained at about 50 ps.

The quality factor Q of this circuit (Figure 5) can be expressed as (Agrwal 2001)

$$Q = \frac{P_1 - P_0}{\sigma_1 + \sigma_0} \tag{7}$$

Here $P_1(P_0)$ and $\sigma_1(\sigma_0)$ are, respectively, the average power and standard deviation of the circuit outputs at high state (0's state). So

$$P_1 = \frac{1}{n}\sum_{i=1}^{n} P_{out,i} \tag{8}$$

where n is the number of output terminals that is in one state and $P_{out,i}$ is corresponding value of output.

$$P_0 = \frac{1}{m}\sum_{j=1}^{m} P_{out,j} \tag{9}$$

where m is the number of output terminals that is in zero state and $P_{out,j}$ is the corresponding value of output. The values of σ_1 and σ_0 are calculated from the following equations.

$$\sigma_1 = \sqrt{\frac{\sum_{i=1}^{n}(P_{out,i} - P_1)^2}{n}} \tag{10}$$

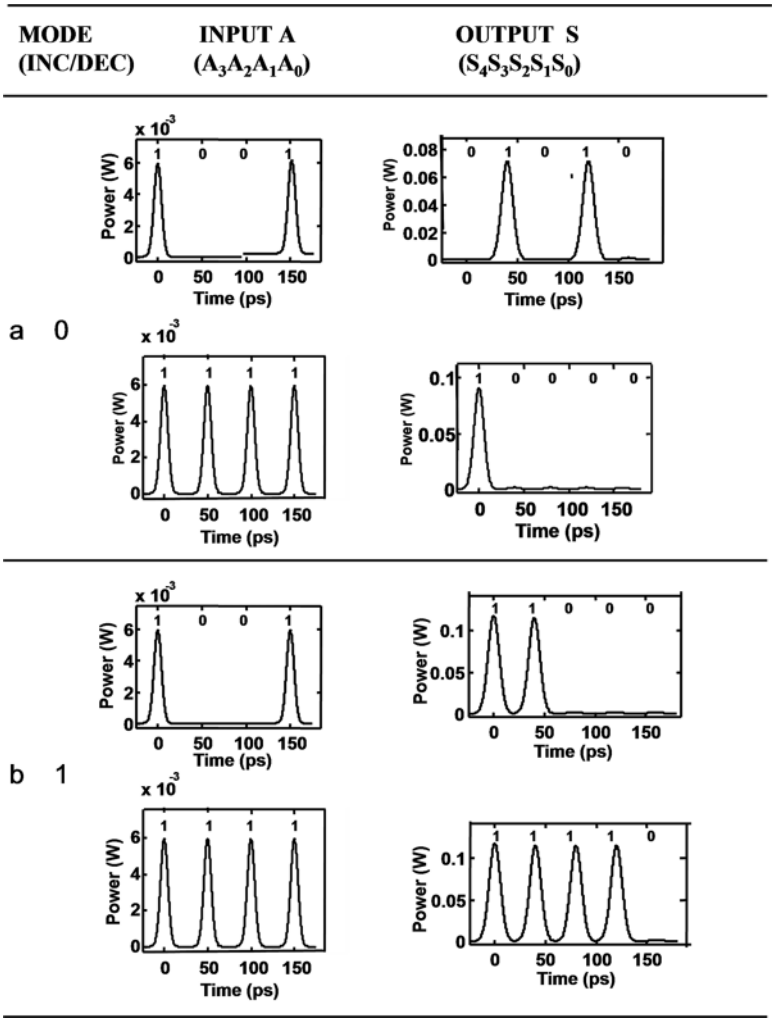

Figure 10. Simulated waveform of incrementer/decrementer.

$$\sigma_0 = \sqrt{\frac{\sum_{j=1}^{m} (P_{out,j} - P_0)^2}{m}} \tag{11}$$

Also bit error rate (*BER*) is obtained from the formula:<EQ>

$$BER = \frac{1}{2} erfc\left(\frac{Q}{\sqrt{2}}\right) = \frac{\exp(-Q^2/2)}{Q\sqrt{2\pi}} \tag{12}$$

'*erfc*' is complimentary error function. We plot the *BER* against different values of the control pulse energy (E_{cp}) and as shown in Figure 14. We get bit error rate about

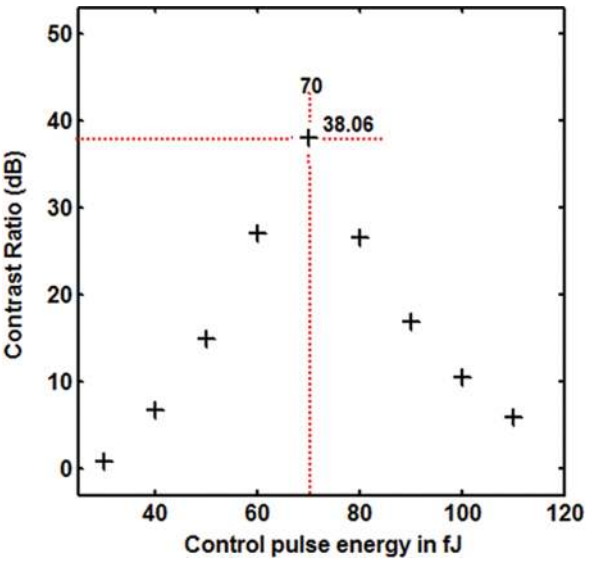

Figure 11. The variation of contrast ratio (*C.R.*) with control pulse energy (E_{cp}) in the output of Figure 5.

10^{-7} which is greater than the bit error rate that are found in stage 1 and stage 2. Bit error rate increases as the number of stages are increased.

Using the operation conditions, we get the contrast ratio and bit error rate are 38.06 dB, and nearly 10^{-7}, respectively, which are more adequate for all-optical logic applications. The P^1_{Min} and P^0_{Max} are connected to the line-width enhancement factor α as

$$\frac{P^0_{Max}}{P^1_{Min}} = \left(1 - e^{-\pi/\alpha}\right)^2 \tag{13}$$

Solving this equation for α, we obtain

$$\alpha = \frac{-\pi}{\ln\left(1 - \sqrt{\frac{P^0_{Max}}{P^1_{Min}}}\right)}. \tag{14}$$

With these input combinations the circuit gives the value of $P^0_{Max} = 0.0438\,\text{W}$ and $P^1_{Min} = 0.0016\,\text{W}$. Then using (14), we obtain $\alpha = 6.43$. The design of the all-optical circuit is presented. Some important issues and the usefulness of this scheme are discussed as follows.

The simulation results demonstrate that although the performance of our proposed model is adequate to perform all-optical incrementer/decrementer operation, the parameters of interest include the SOA small signal gain, line-width enhancement factor and carrier lifetime, the control pulses energy and width, and the loop asymmetry. Among these parameters, the energy of the control pulses is of particular importance because it determines the degree of the SOA gain saturation

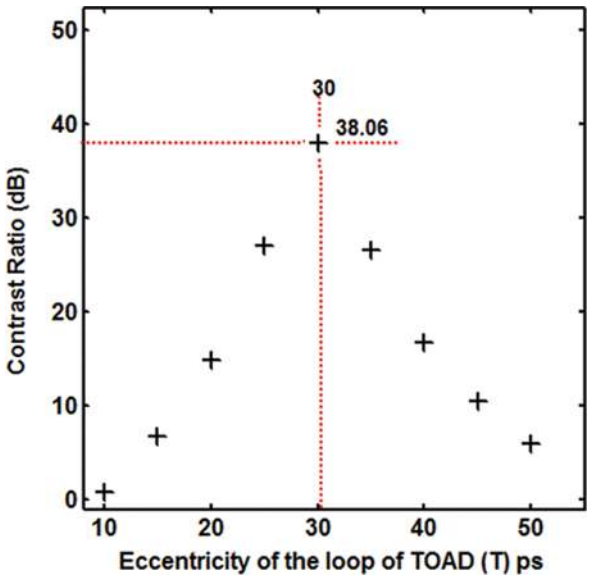

Figure 12. Variation of contrast ratio (*C.R.*) with Eccentricity of the loop (T) of TOAD in the output of Figure 5.

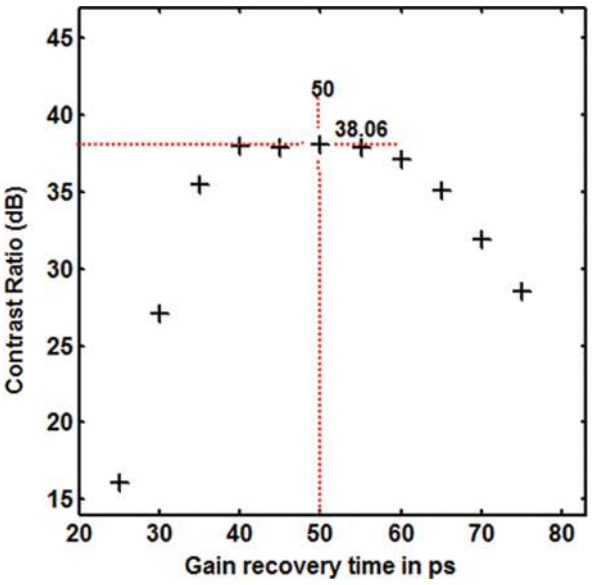

Figure 13. Variation of contrast ratio (*C.R.*) with gain recovery time (τ_e) in the output of Figure 5.

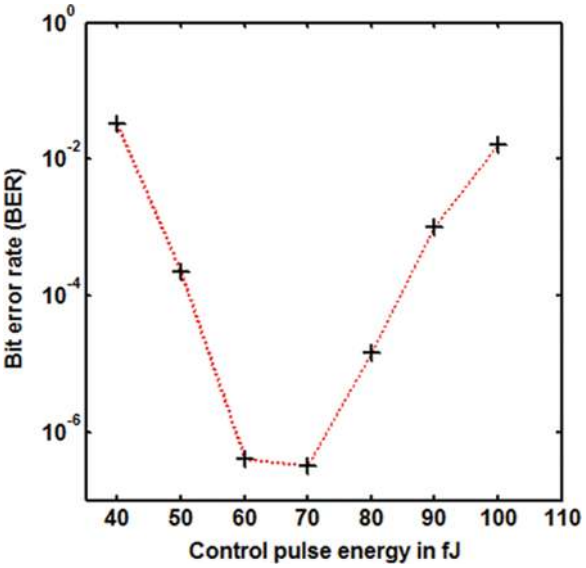

Figure 14. The variation of bit error ratio (BER) with control pulse energy (E_{cp}) in the output of Figure 5.

required for optimum operation. At the same time it must be kept as low as possible. So we take control pulse energy in the range 60–80 fJ. We choose small signal gain as $G_{ss} = 20$ dB. The reason for this is that higher small signal gain values affect drastically the SOA dynamics. When the value of small signal gain increased, the stronger the SOA is saturated and the less is its gain dependent on the pulse energy. So 70 fJ per control pulse must be ideally provided to obtain the highest contrast. The SOA carrier lifetime is a key operational factor that affects decisively the performance of the optical circuit. SOA gain recovery time is one of the important parameters for high speed photonics logic operation. As a consequence, major improvement in performance of conventional bulk SOAs are required, which can be achieved by deploying successfully tested gain recovery reduction techniques. An alternative solution in order to meet the higher speed requirements is to exploit the novel technology of quantum dot SOAs and take advantage of its attractive operational features and ultra-fast gain dynamics to perform ultra-high speed all-optical processing. The carrier lifetime must be reduced so that it is smaller than the specific bit period and the gain can recover completely between consecutive pulses. So we choose carrier lifetime $\tau_e = 50$ ps. The eccentricity of the loop must be chosen carefully, here we take $T = 30$ ps, when it approaches the upper limit value of carrier lifetime a better performance is achieved. This happens because in that case the CCW clock pulse is appropriately delayed with respect to its CW counterpart so that a sufficient gain and phase difference can be created independently. We choose full width at half maximum of control pulse (T_{FWHM}) = 3.33 ps. The small value of line-width enhancement is necessary in order to obtain a high contrast. For this reason we choose line-width enhancement $\alpha = 6$.

6. CONCLUSION

In this article we have reported a novel design of TOAD-based incrementer/decrementer. Here, in this proposed scheme the significant advantage is that the proposed circuit can perform INC/DEC operations, which are all-optical in nature. This scheme can easily and successfully be extended and implemented for any higher number of input digits by proper incorporation of TOAD-based switches. Numerical simulation results confirming the described method are given in this article. The variation of contrast ratio with different values of control pulse energy, eccentricity of the loop, gain recovery time at different stages, and at the output has been thoroughly investigated. The variation of bit error with different values of control pulse energy at different stages and at the output also has been thoroughly investigated. In our proposed design we determine the contrast ratio and bit error rate as 38.06 dB and nearly 10^{-7}, respectively, which are more adequate for all-optical logic based information processing systems.

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